

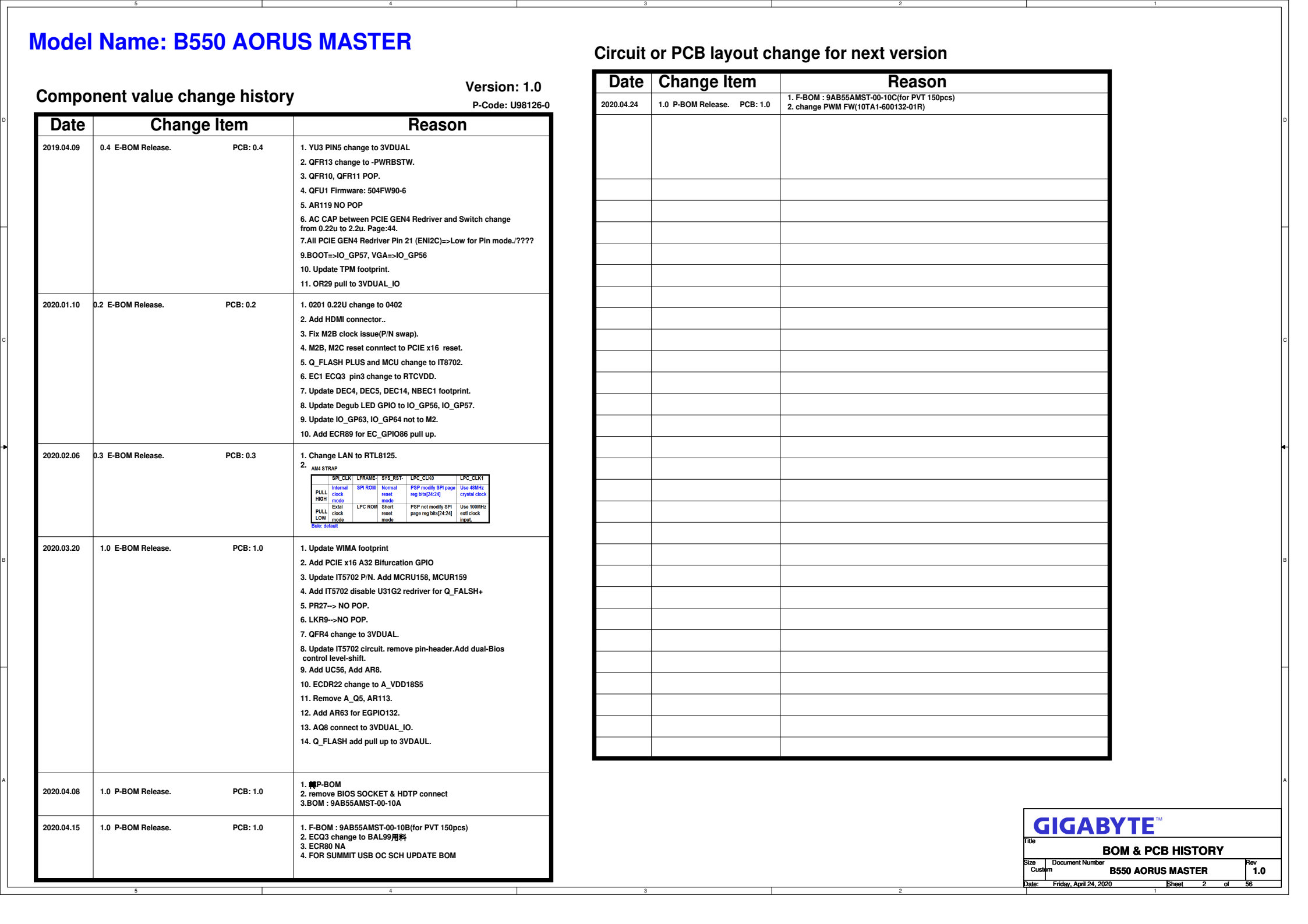
B550 AORUS MASTER

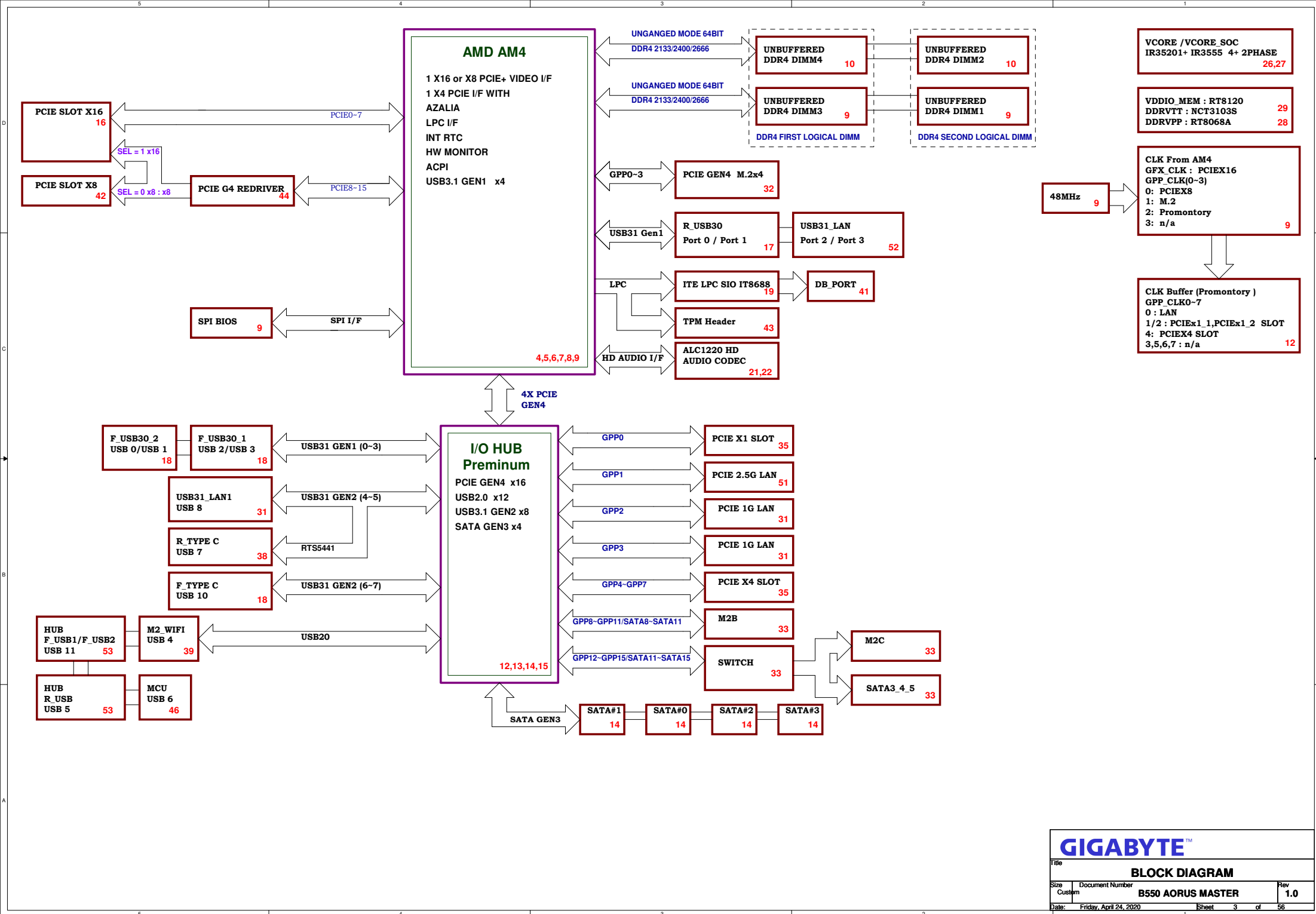
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22	AUDIO JACK	
23	ATX , FRONT PANEL	
24	POWER SEQUENCE	
25	PWM IR35201	

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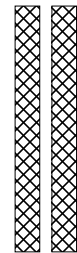
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Model Name: B550 AORUS MASTER																																																																	
Component value change history			Version: 1.0 P-Code: U98126-0																																																														
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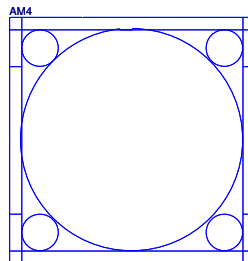
[illegible][illegible][illegible][illegible][illegible]



MEM CHA



<10> MODT_A[0..3] ↔ MODT_A[0..3]
<10> MDA[0..63] ↔ MDA[0..63]
<10> MAAA[0..16] ↔ MAAA[0..16]
<10> DQSA[0..8] ↔ DQSA[0..8]
<10> -DQSA[0..8] ↔ -DQSA[0..8]



AM3RM/SC/BL/MB[12KRC-04K813-12R_12KRC-04K813-14R]

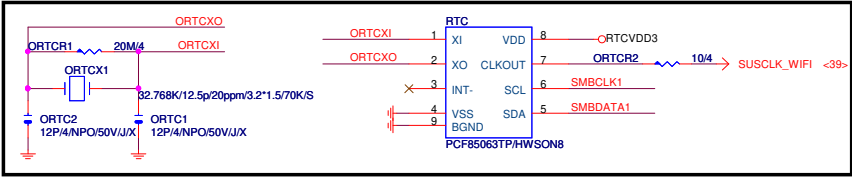
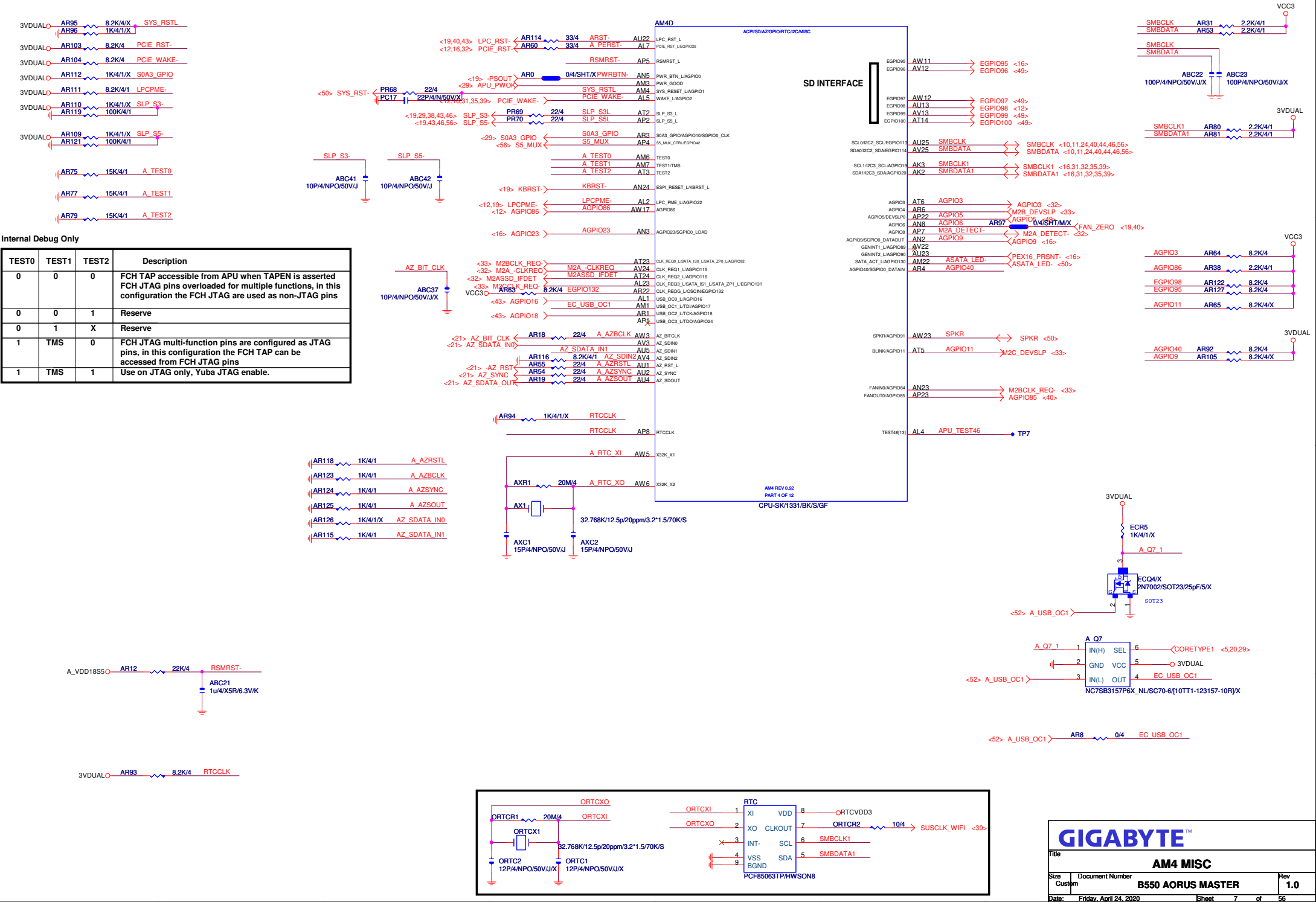
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Title			APU DDR4		
Size	Document Number	B550 AORUS MASTER			Rev
Custom					1.0
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Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



GIGABYTETM

AM4 MISC

Document Number
B550 AORUS MASTER

Rev
1.0

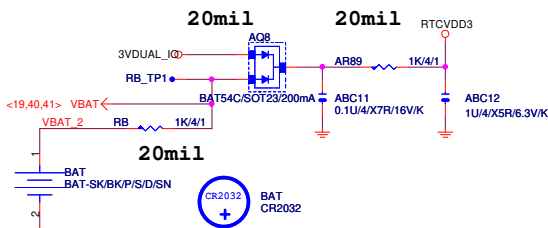
Title
AM4 MISC


Size
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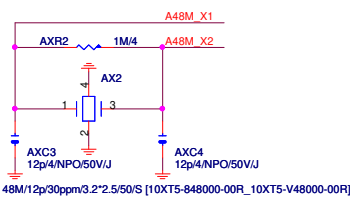
Date
Friday, April 24, 2020

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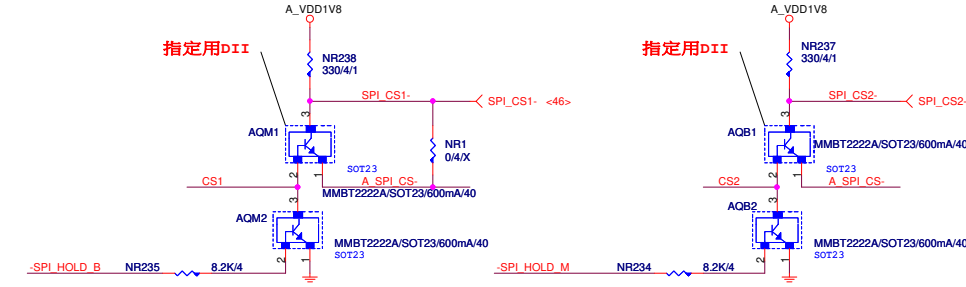
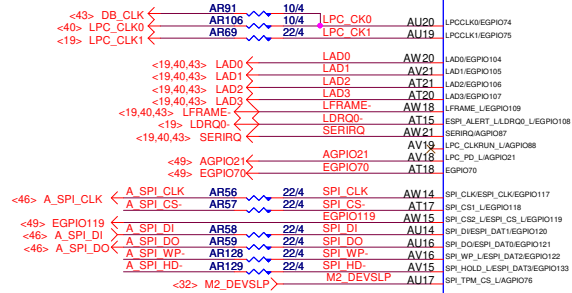
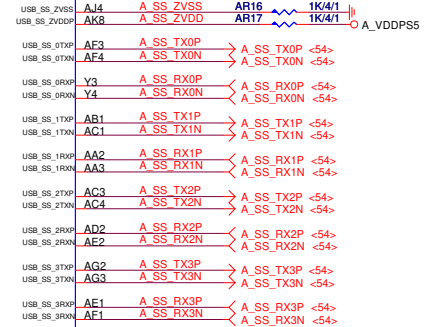
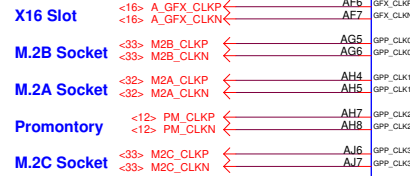
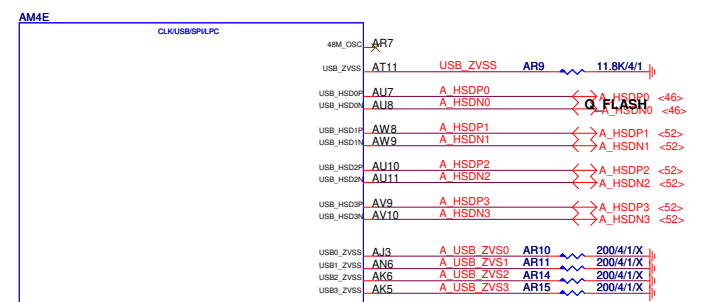
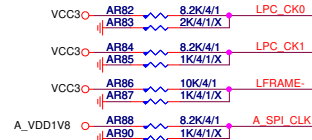
				
Title				
CPU POWER & GND				
Size Custom	Document Number B550 AORUS MASTER	Rev 1.0		
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AM4 STRAP

	SPI_CLK	LFRAME-	SYS_RST-	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.

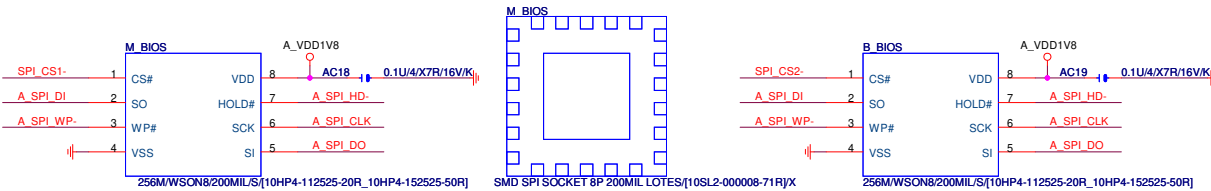
Bule: default



★1.8V SPI ROM USE



Fix flash BIOS fail Issue 1K to 330 ohm



GIGABYTE™

APU USB, GPP

Size: Custom

Document Number: B550 AORUS MASTER

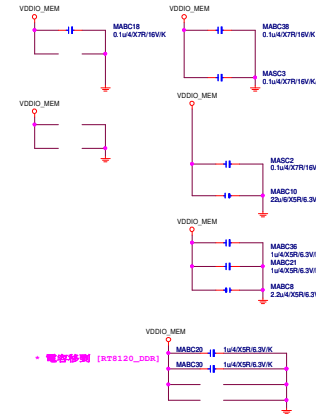
Date: Friday, April 24, 2020

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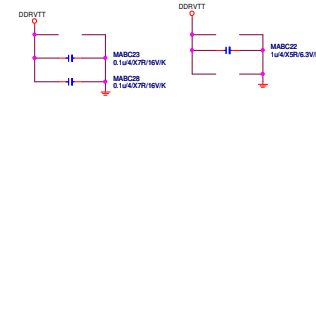
Rev: 1.0

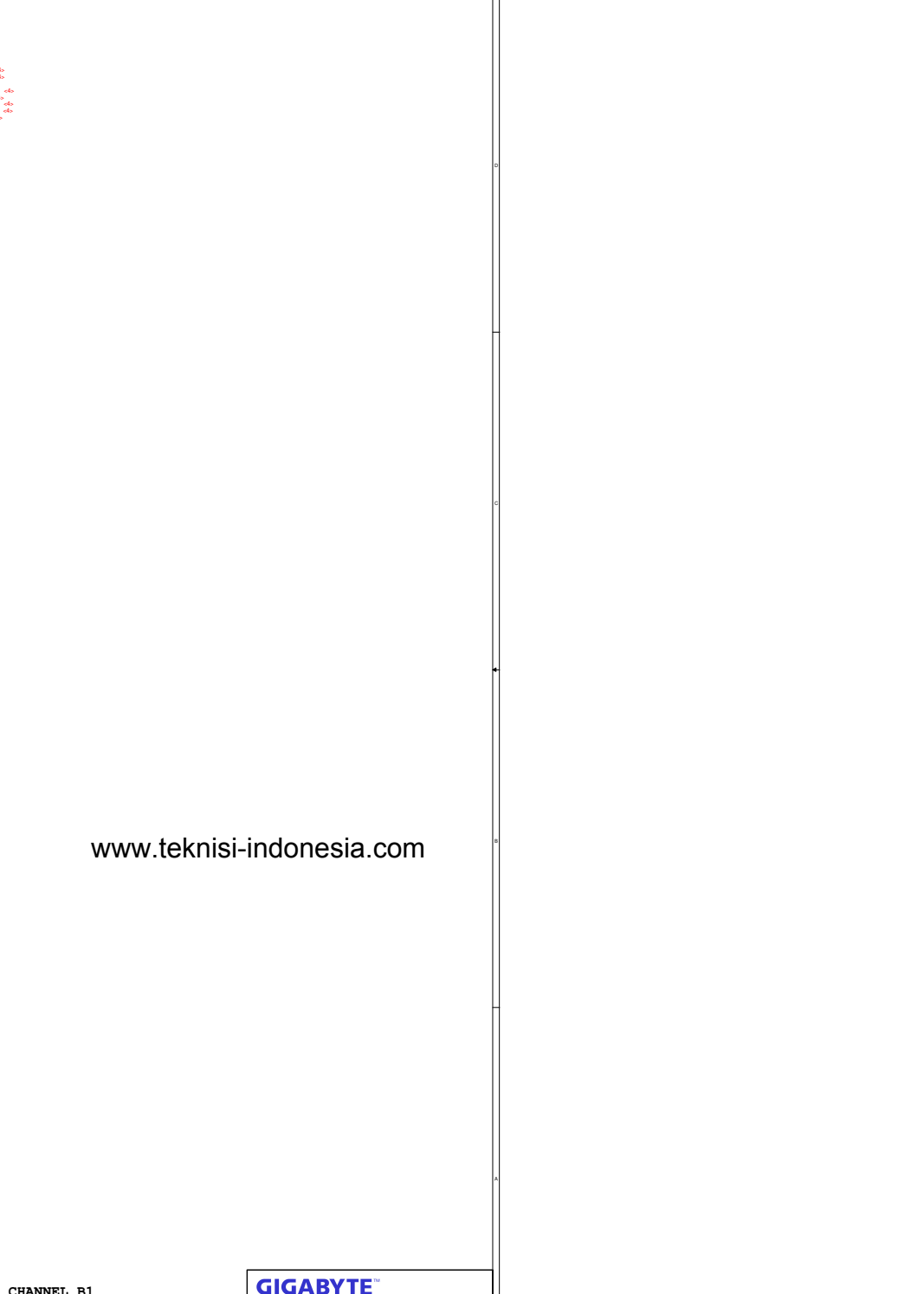


DDR12V Decouple



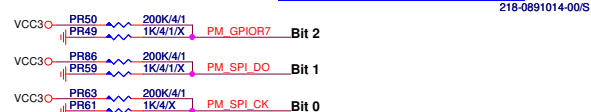
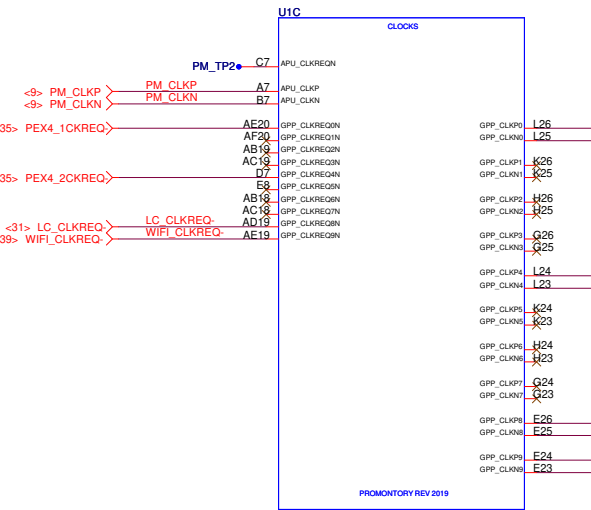
DDRVRTT Decouple



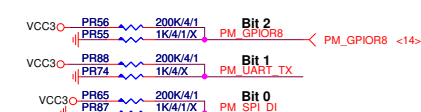


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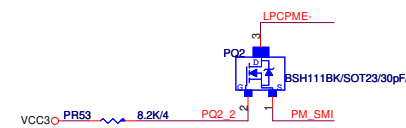
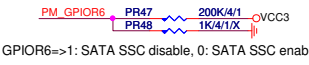
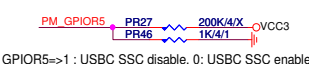
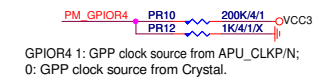
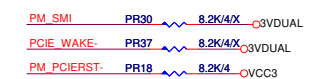
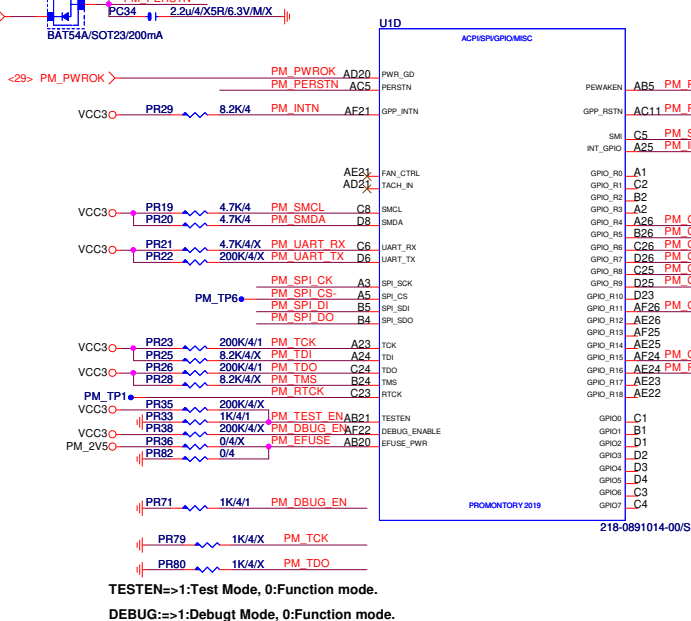
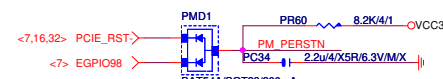
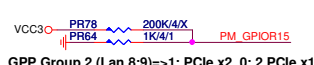
GIGABYTE		
DDR4 CHANNEL B		
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Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



Bit 2	Bit 1	Bit 0	GPP Group 1 (Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
Others: Reserved			



GIGABYTE™

ANS 7964580

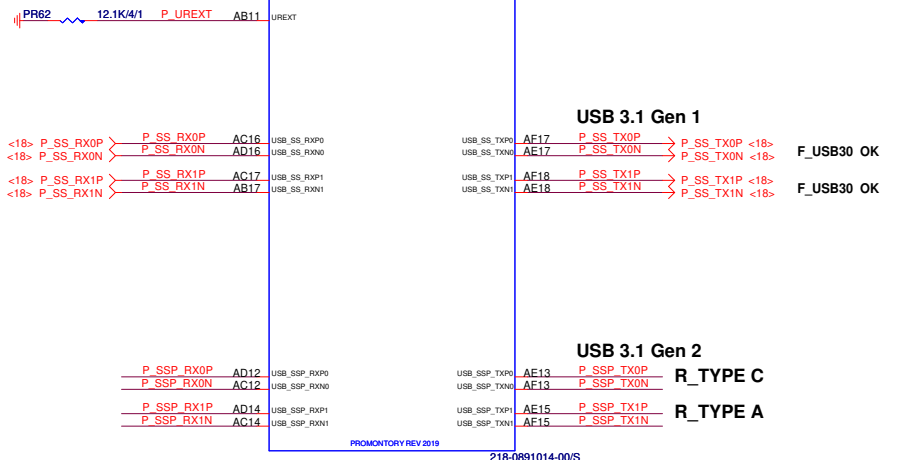
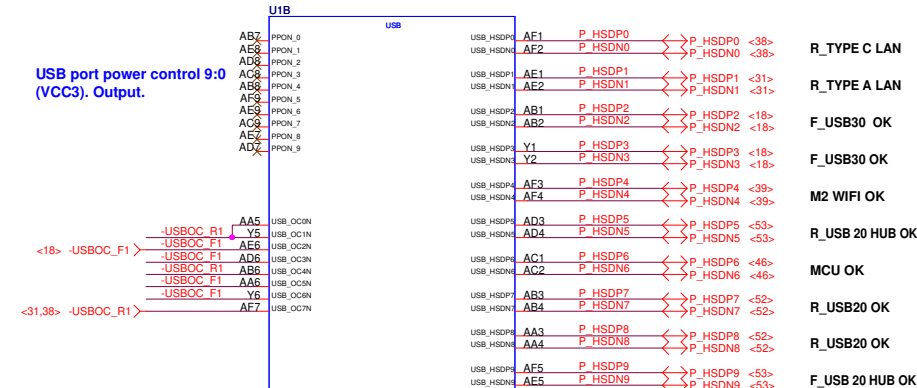
Title

PROMONTORY CPU/CLK/MISC

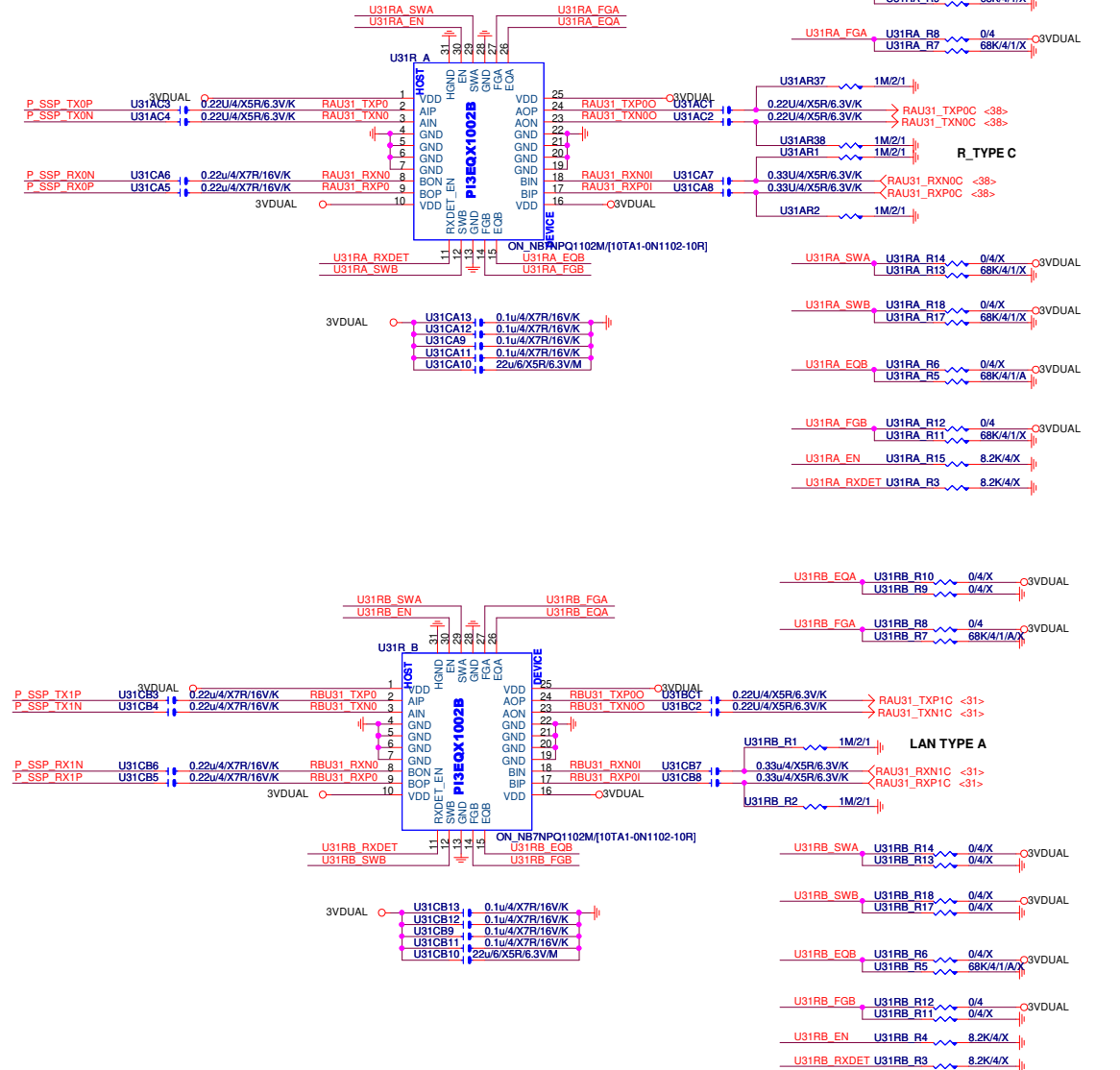
Size Custom Document Number **B550 AORUS MASTER** Rev **1.0**

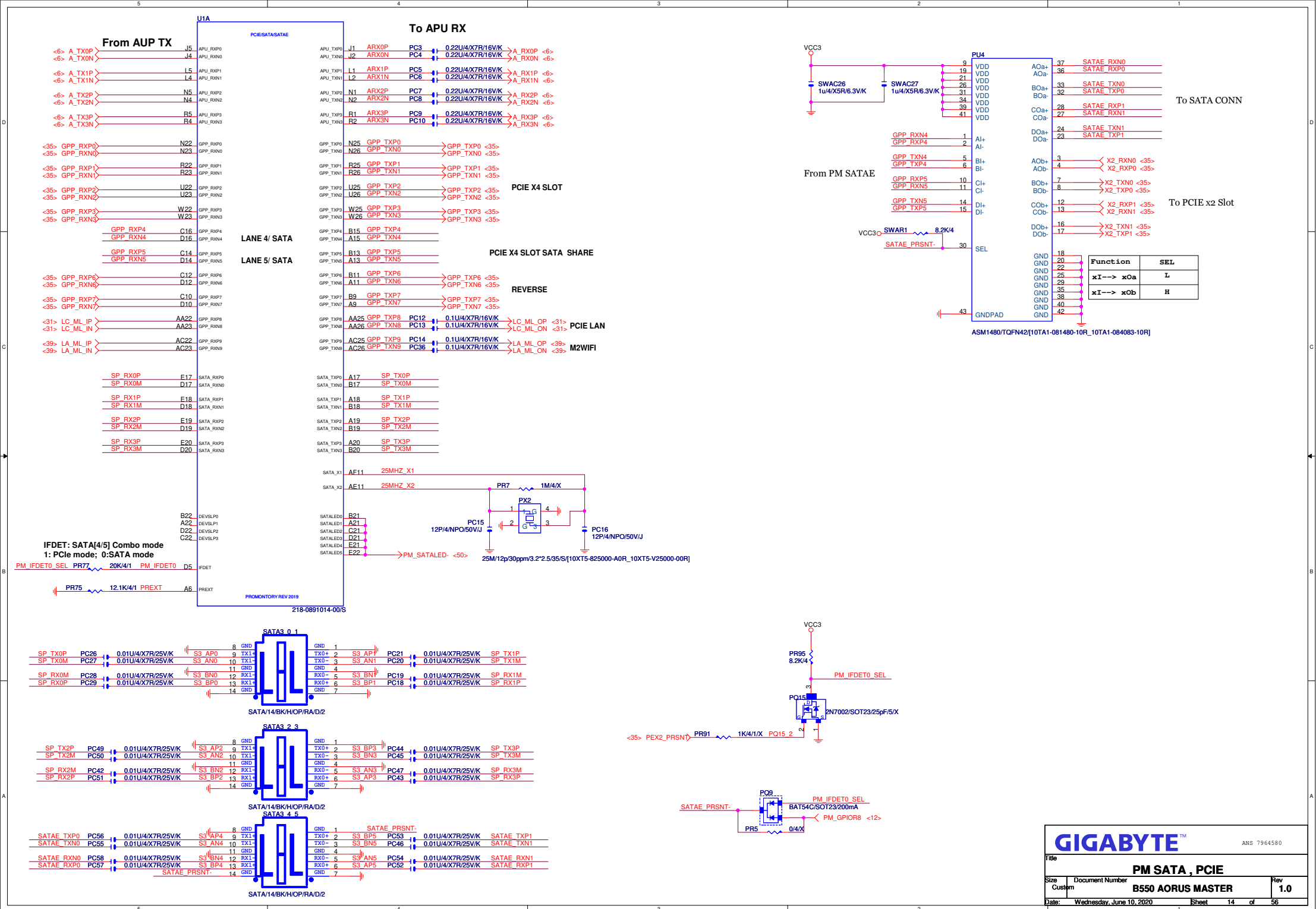
Date: Wednesday, June 10, 2020 Sheet 12 of 56

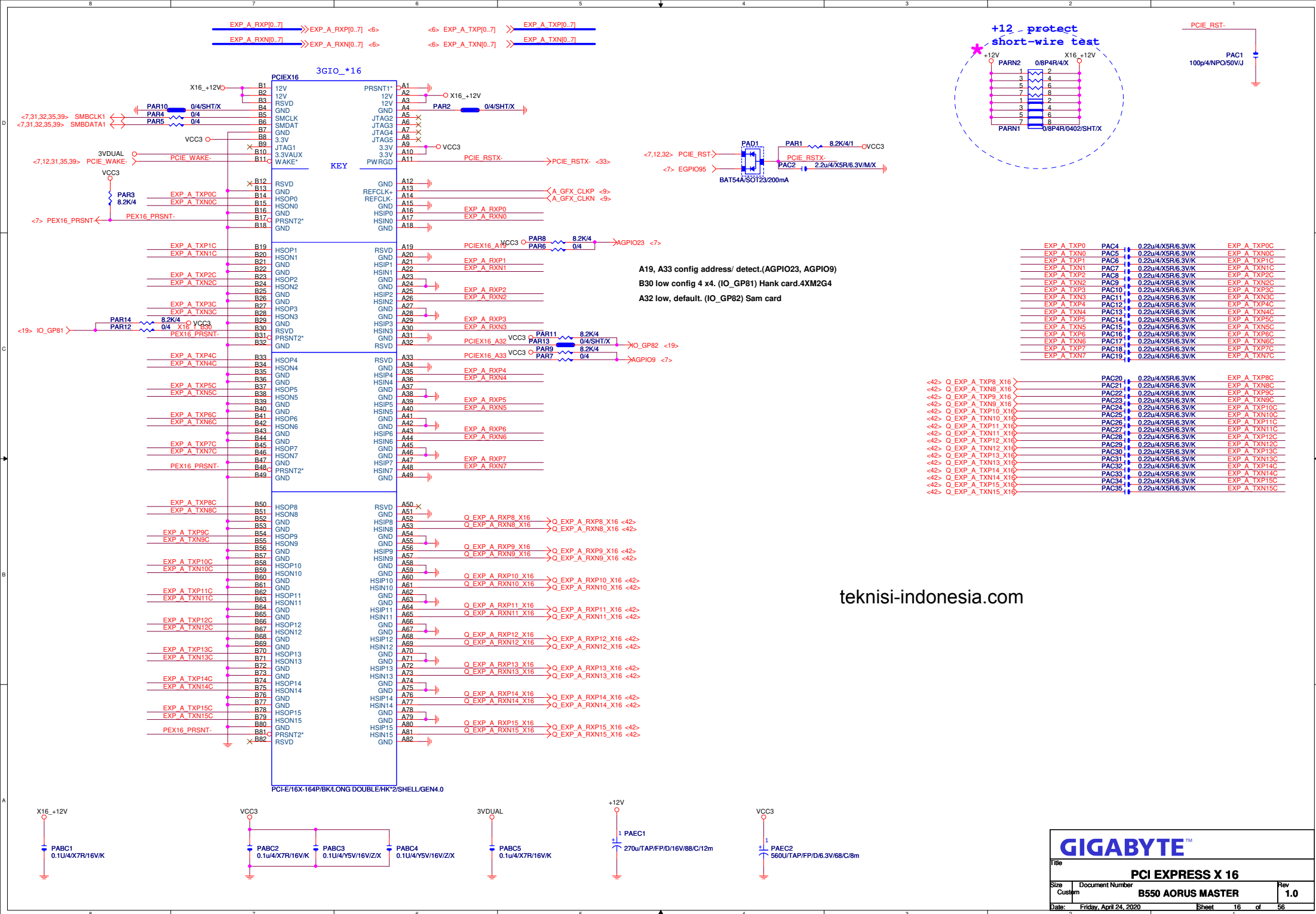
USB port power control 9:0 (VCC3). Output.

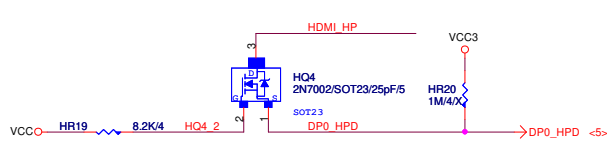
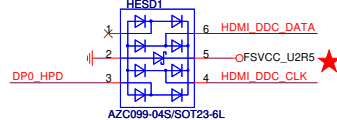
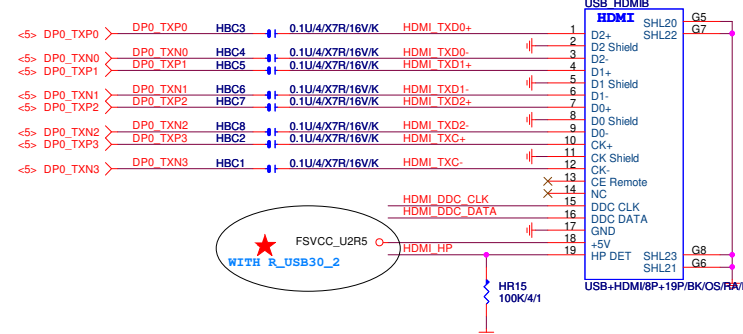
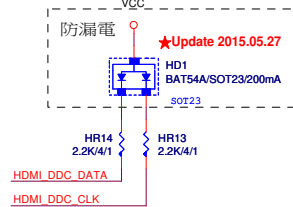
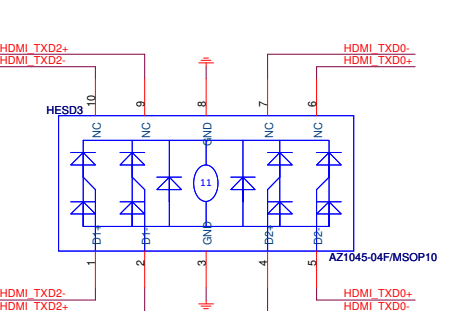
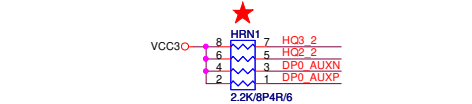
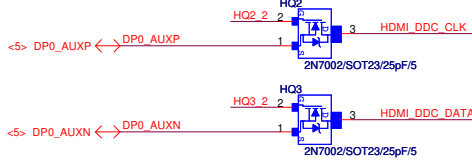
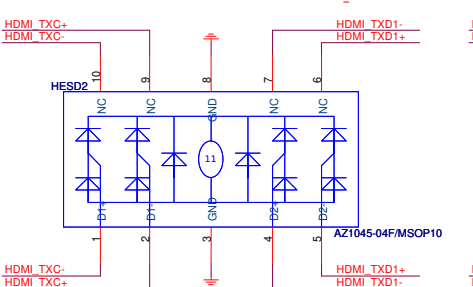
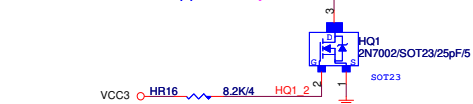
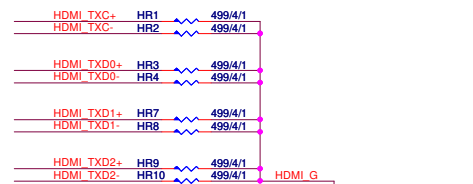


USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7

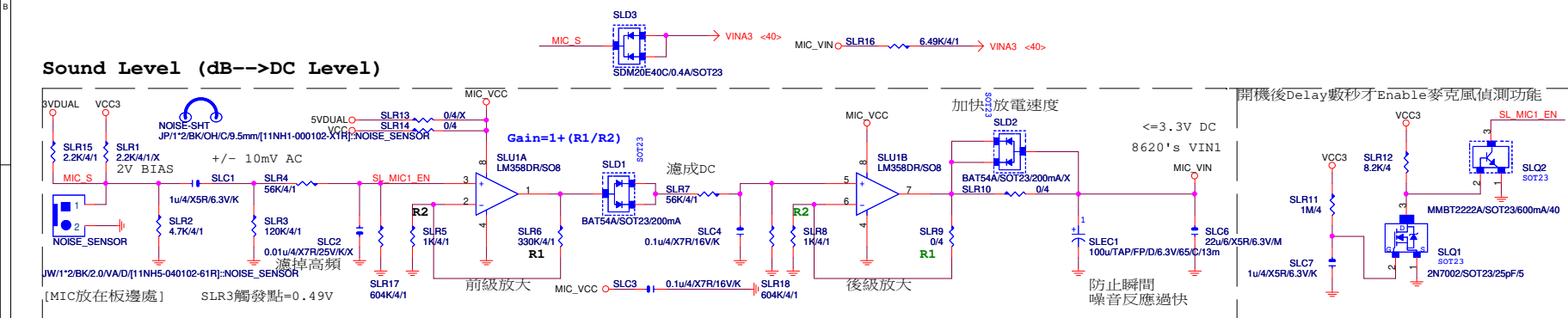
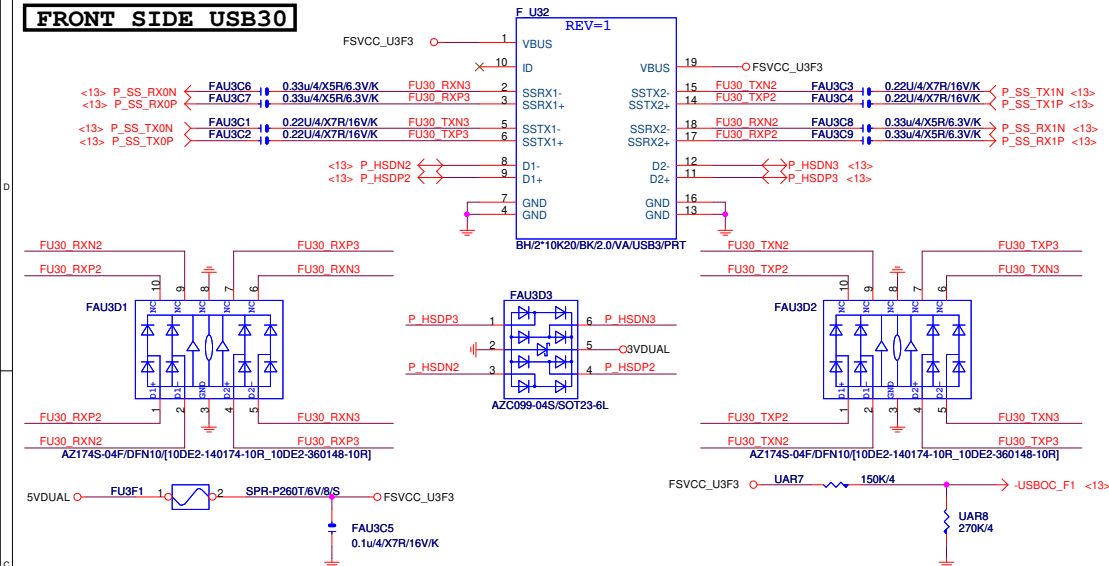


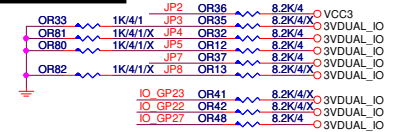
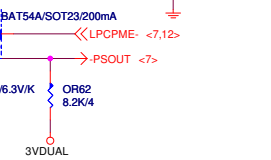
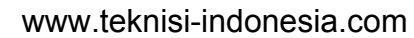






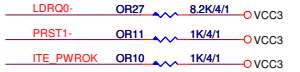
FRONT SIDE USB30





Title			
ITE 8686 LPC IO, TPM, KB/MS			
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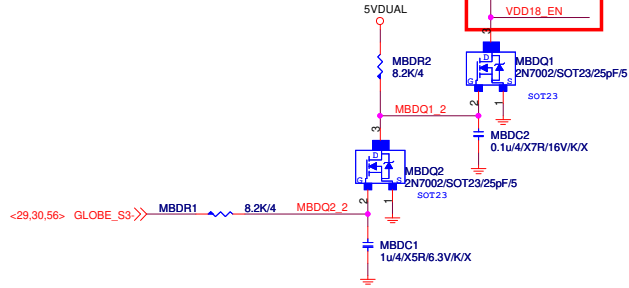
FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89



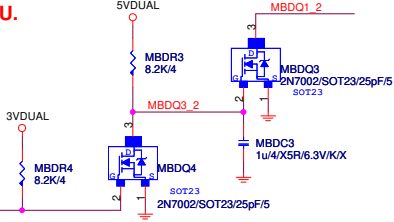
CLOSE SIO PIN4 2_5LEVEL

PWR_SEQ

5VDUAL
上件
MB_DR30
8.2K/4
VDD18_EN

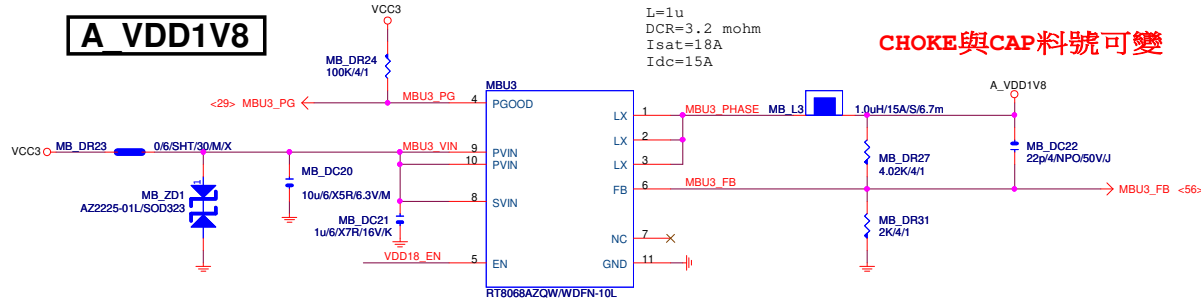


Fix Q_FLASH fail with CPU.

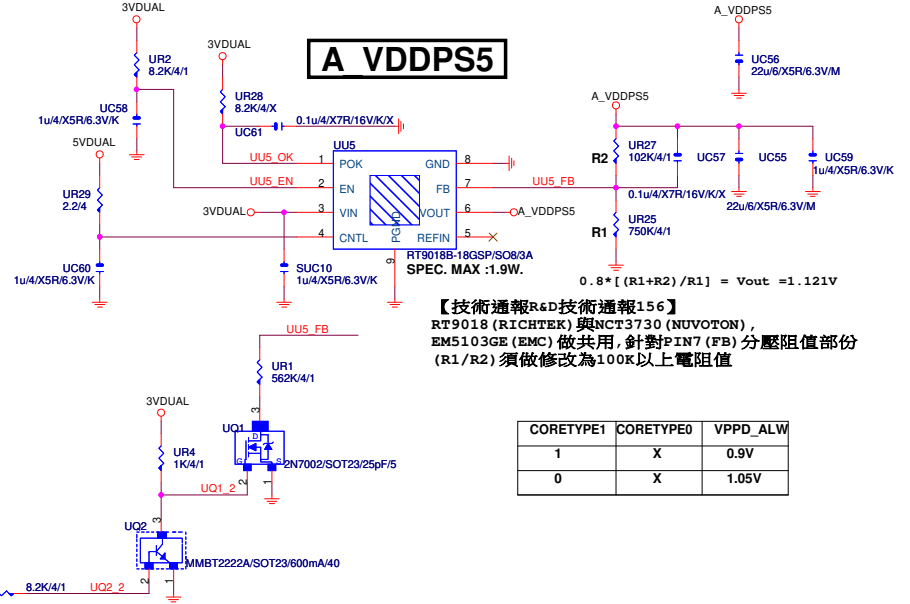


REV:0.4

A VDD1V8



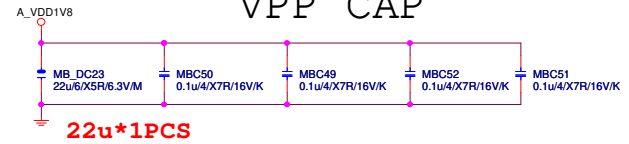
A VDDPS5



【技術通報R&D技術通報156】
RT9018 (RICHTER) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為100K以上電阻值

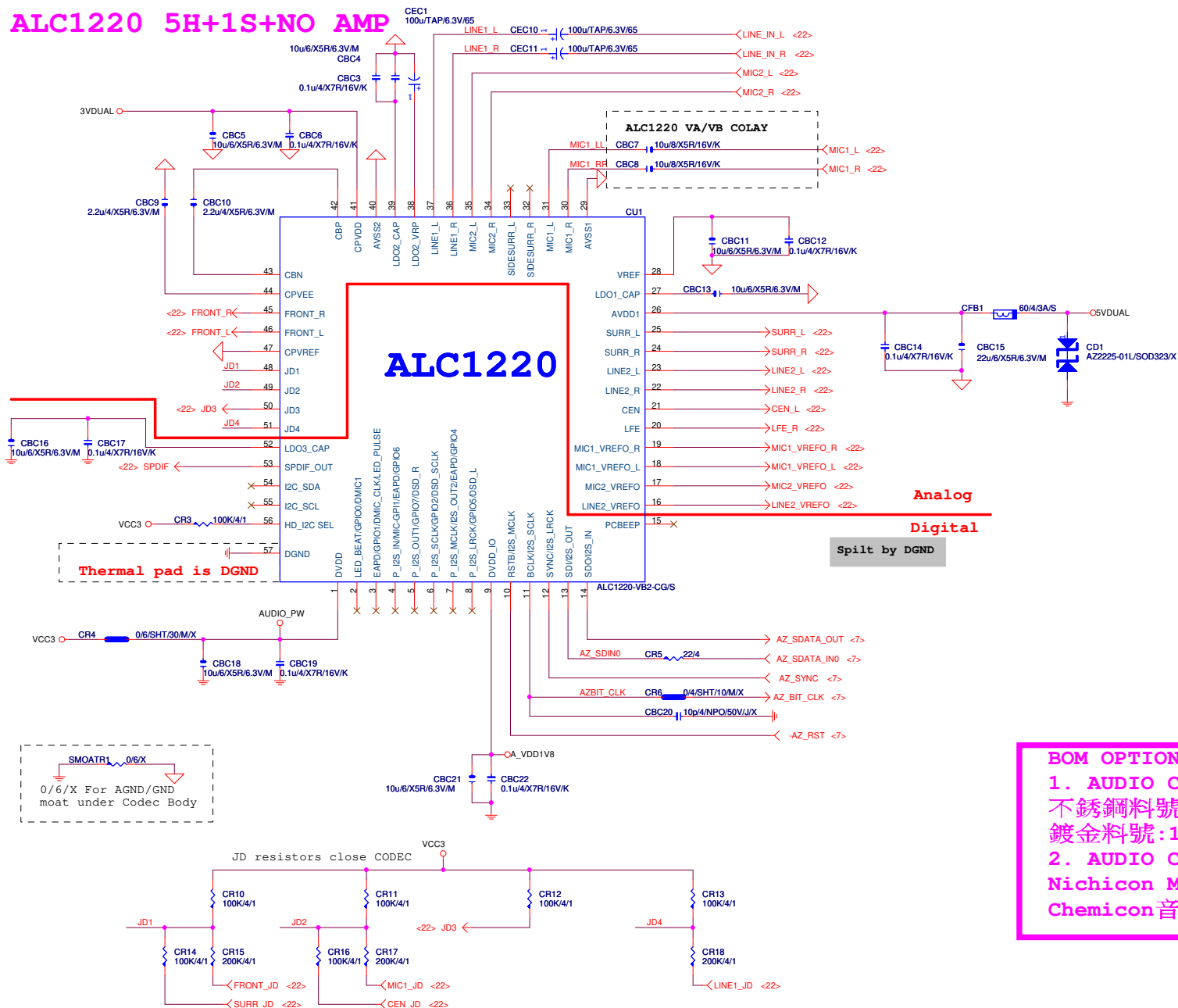
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

VPP CAP



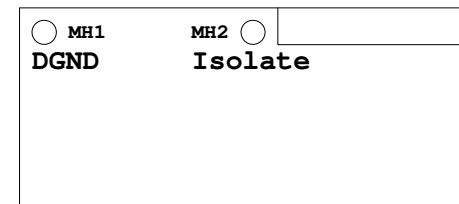
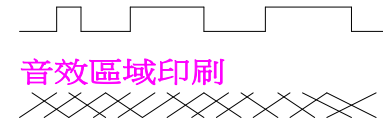
GIGABYTE™		
Title FAN, A_VDD1V8		
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ALC1220 5H+1S+NO AMP



LAYOUT注意: 螺絲孔下GND方式

1. MH1下DGND
2. MH2一律改為Isolate

LAYOUT注意: 是否要加?
AGND切割線

BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號: 11NR6-403025-A3R

鍍金料號: 11NR6-403025-92R

2. AUDIO CAP

Nichicon MW音效電容 : 11CE1-651000-12R

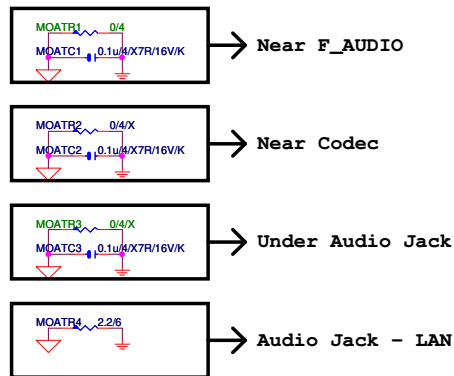
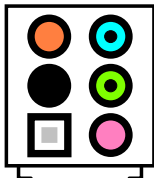
Chemicon音效電容 : 11CE2-651000-05R

GIGABYTE™

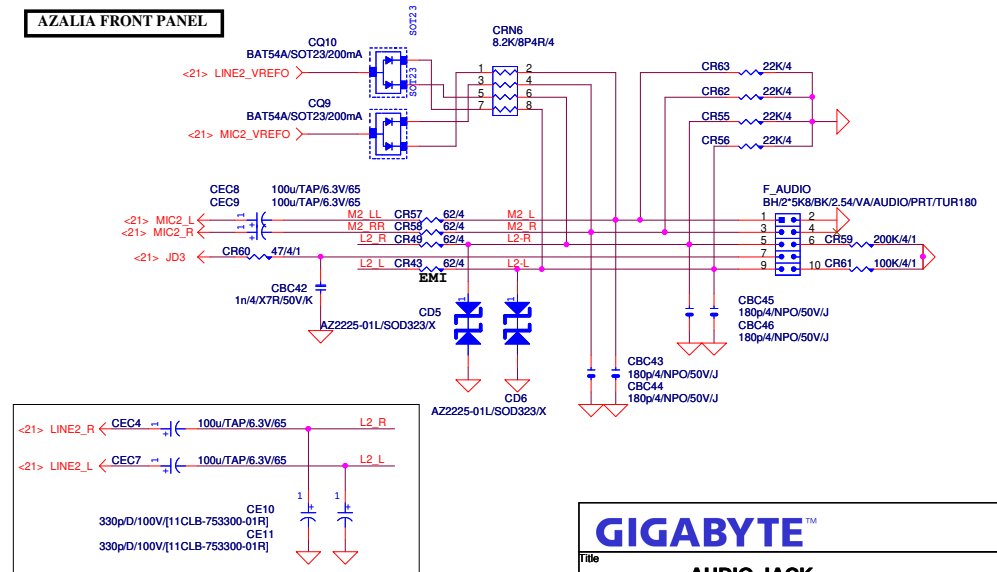
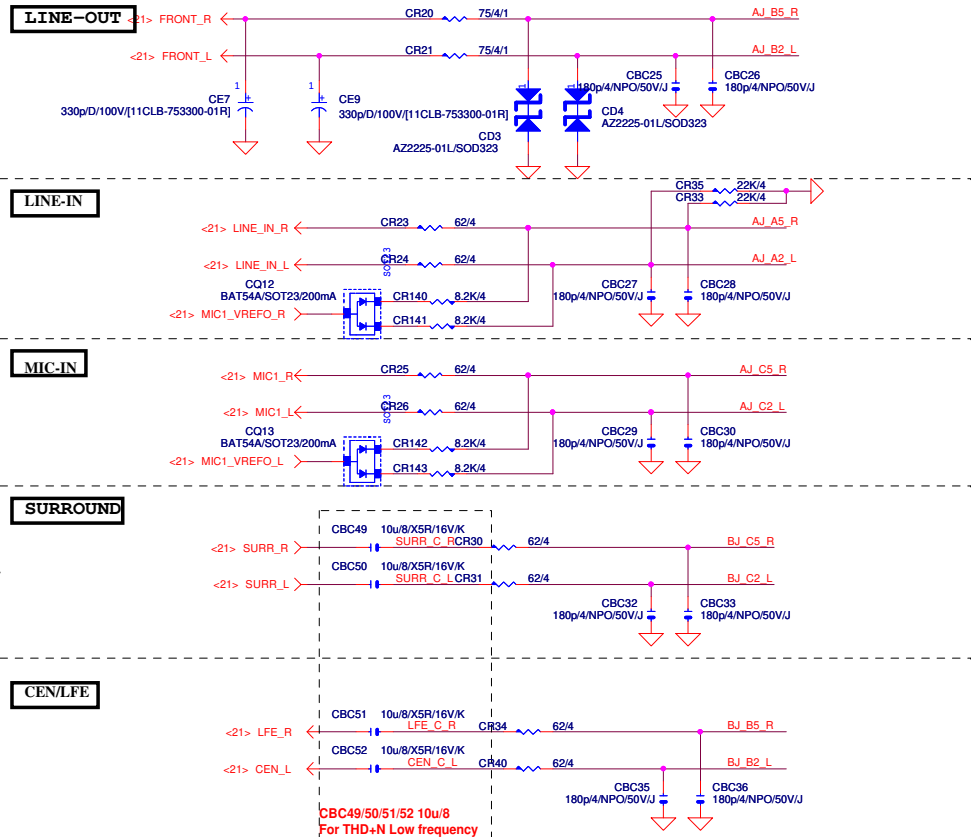
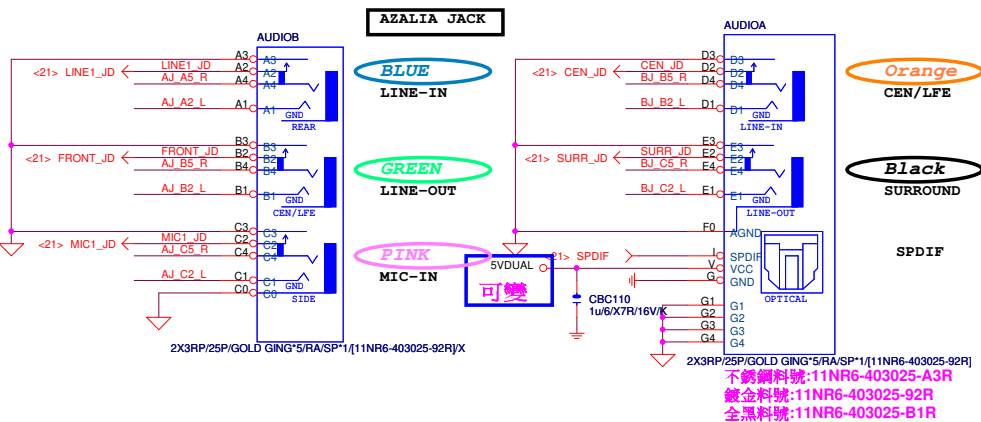
Title			
ALC1220 REAR			
Size	Document Number	Rev	
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Rev 2.05

AZALIA JACK



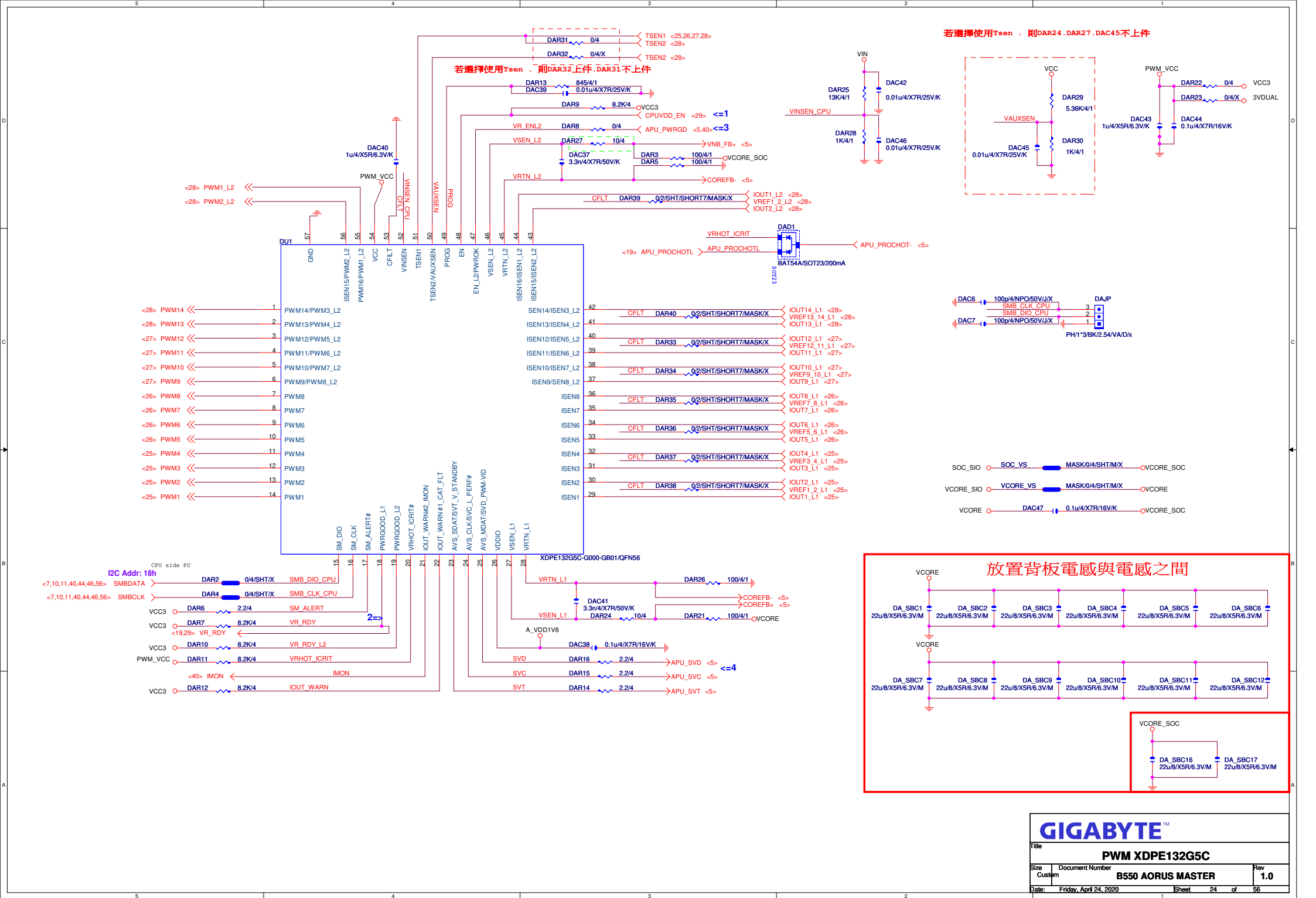
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GIGABYTE™			
Title			
AUDIO JACK			
Size	Document Number	Rev	
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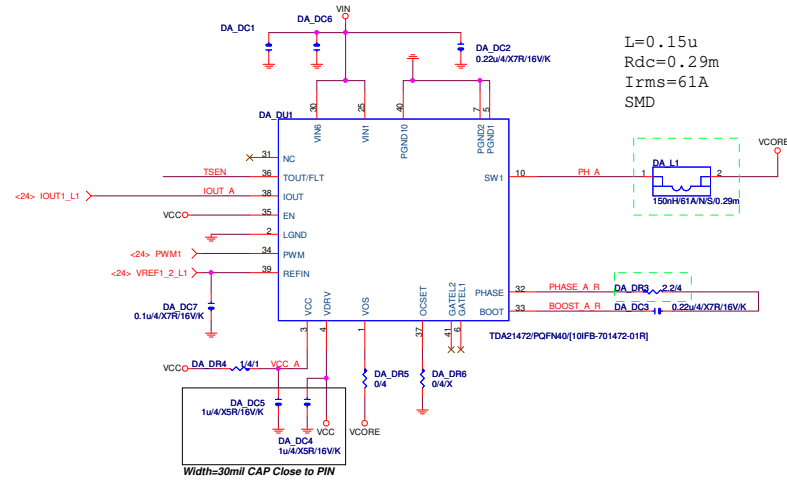
GIGABYTE™			
Title DIGITAL LED			
Size Custom	Document Number B550 AORUS MASTER		Rev 1.0
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REV:0.11

VCORE PHASE1_2

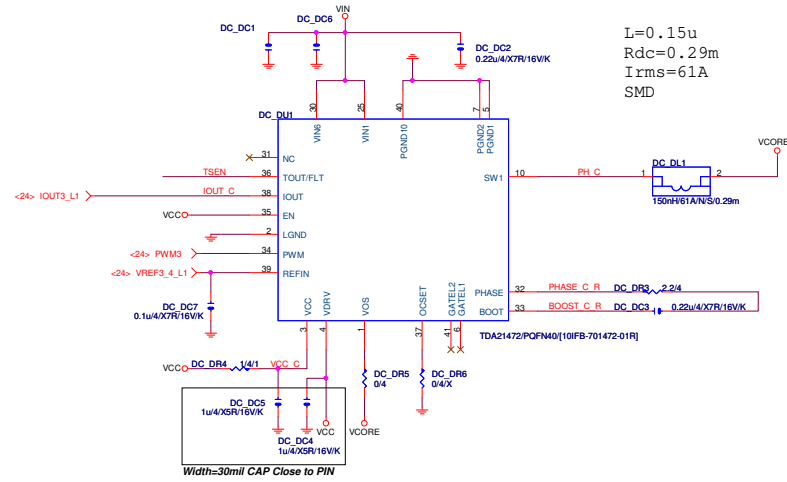
10w/8/X6S/16V/K/[10CM2-3K1005-74R]
10w/8/X6S/16V/K/[10CM2-3K1005-74R]



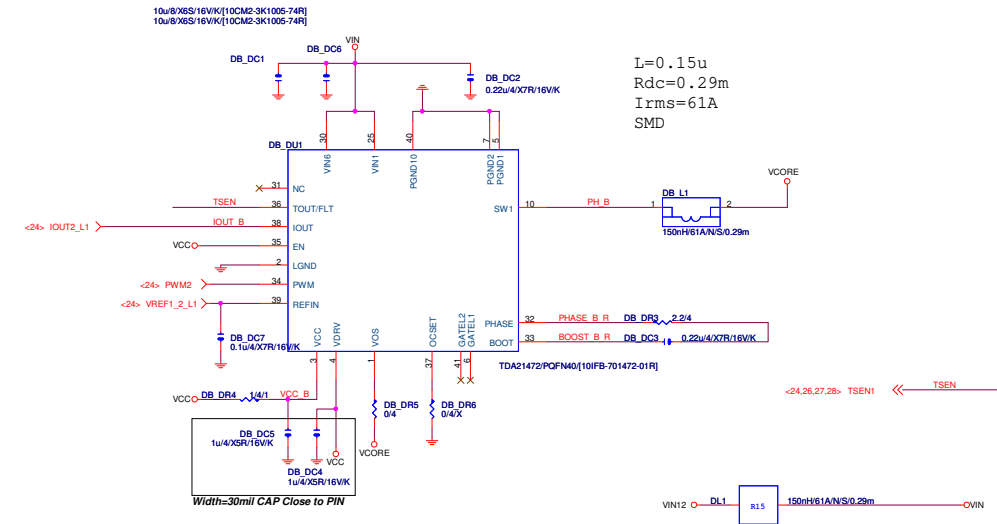
L=0.15u
Rdc=0.29m
I_{rms}=61A
SMD

VCORE PHASE3_4

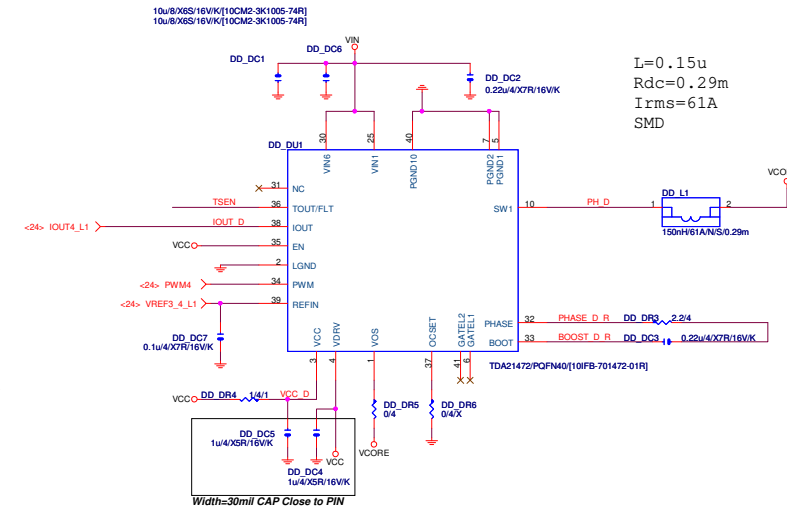
10u/8/X6S/16V/K/[10CM2-3K1005-74R]
10u/8/X6S/16V/K/[10CM2-3K1005-74R]



L=0.15u
Rdc=0.29m
I_{rms}=61A
SMD

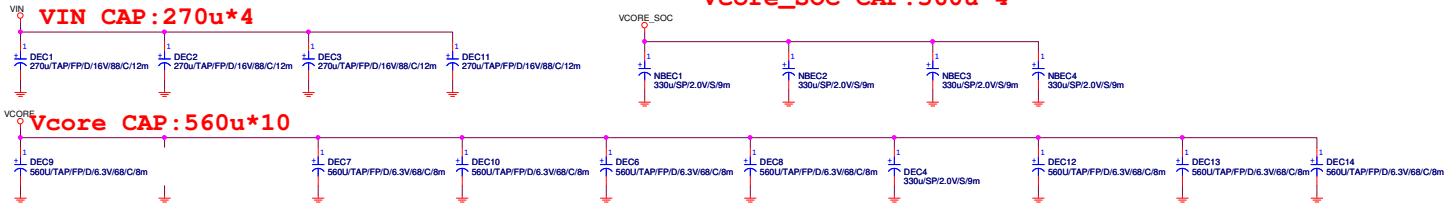


L=0.15u
Rdc=0.29m
Irms=61A
SMD



L=0.15u
Rdc=0.29m
Irms=61A
SMD

Vcore_SOC CAP:560u*4

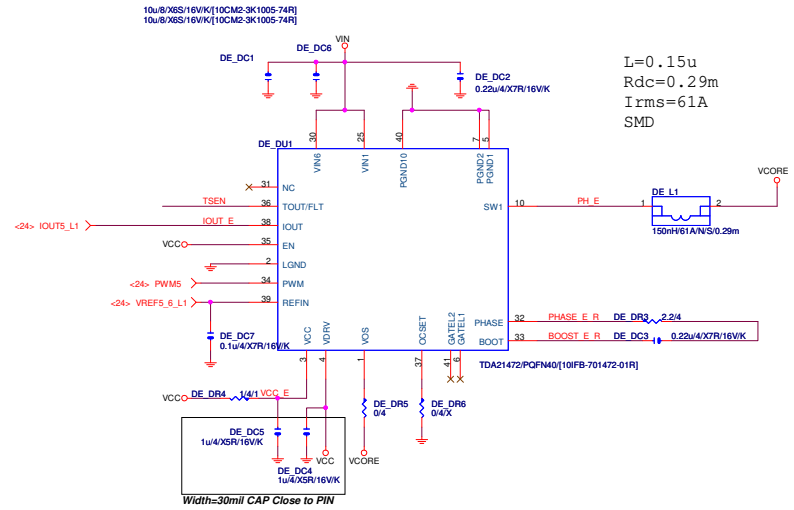


VIN CAP:270u*4

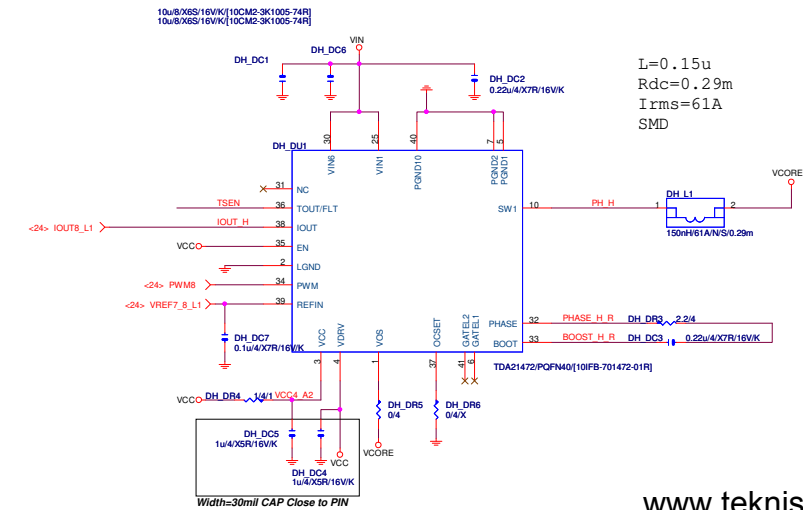
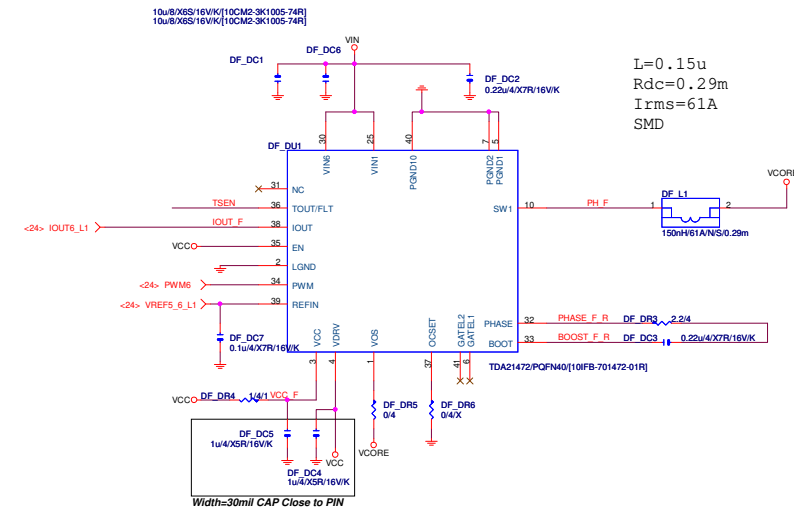
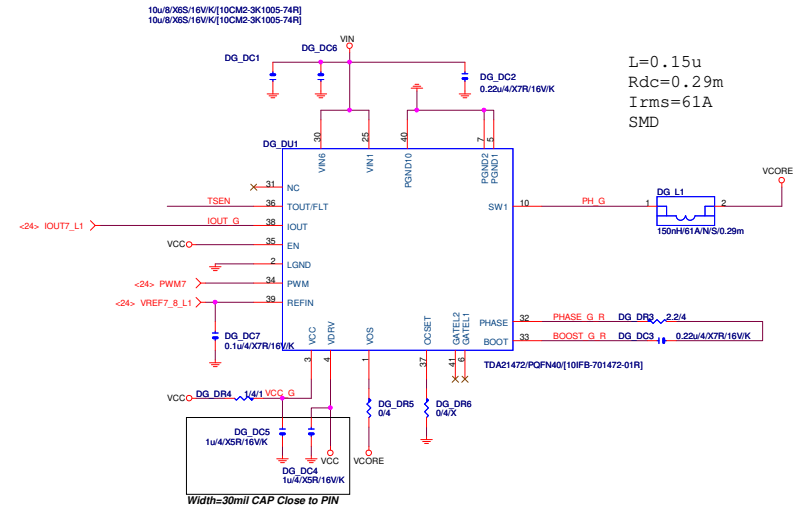
Vcore CAP: 560u*10

REV:0.11

VCORE PHASE5_6



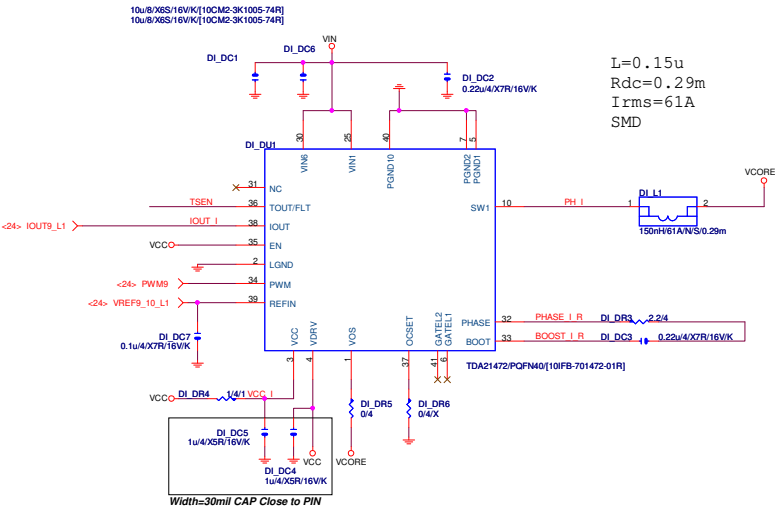
VCORE PHASE7_8



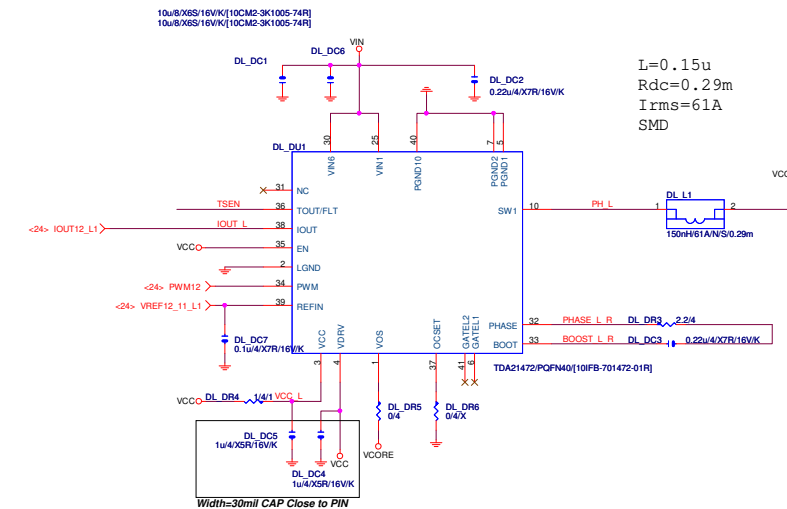
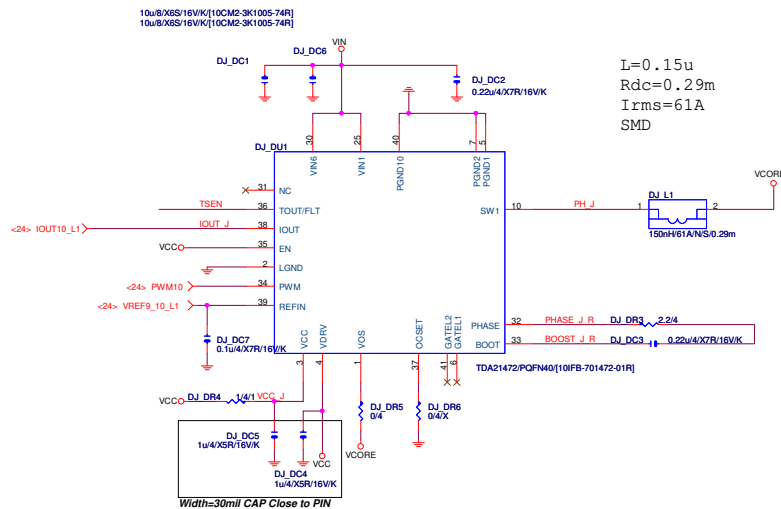
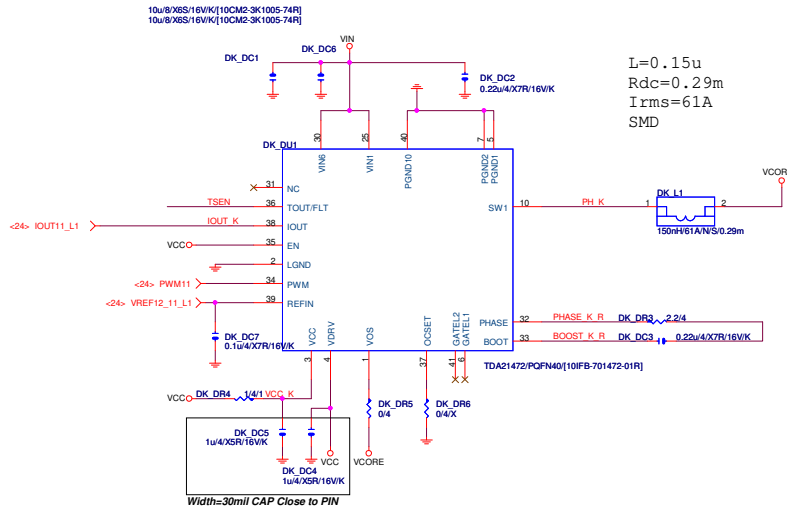
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<24,25,27,28> TSEN << TSEN

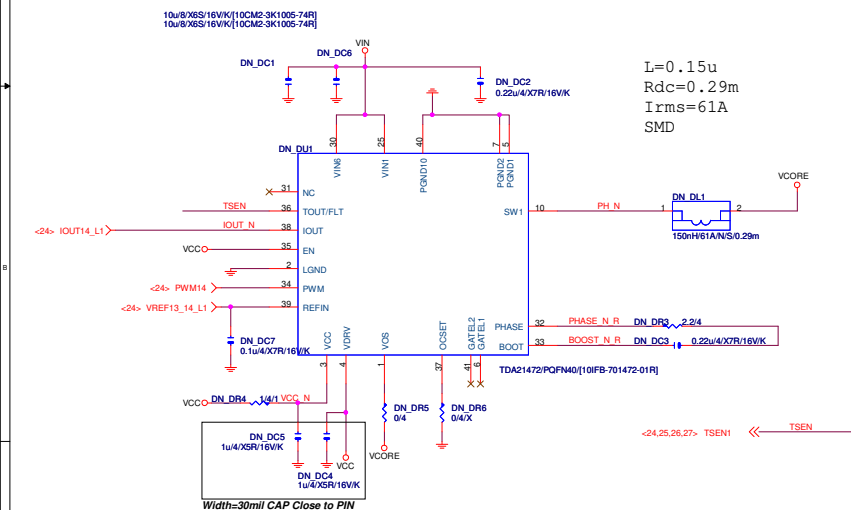
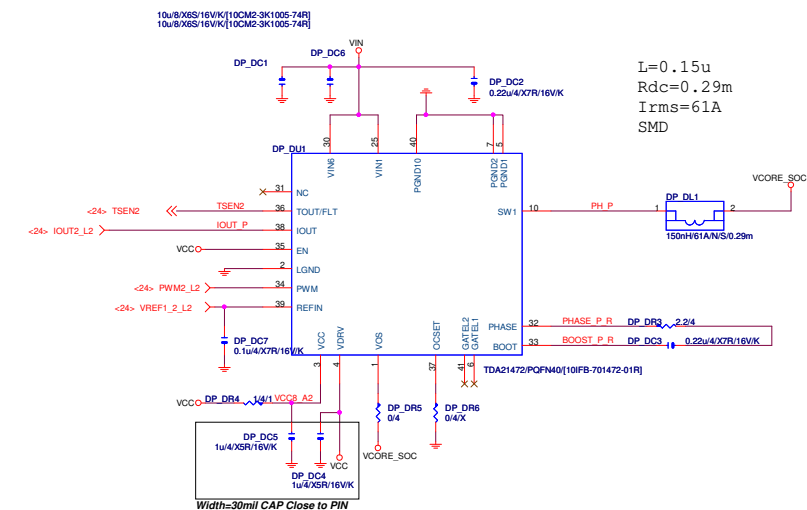
VCORE PHASE9_10

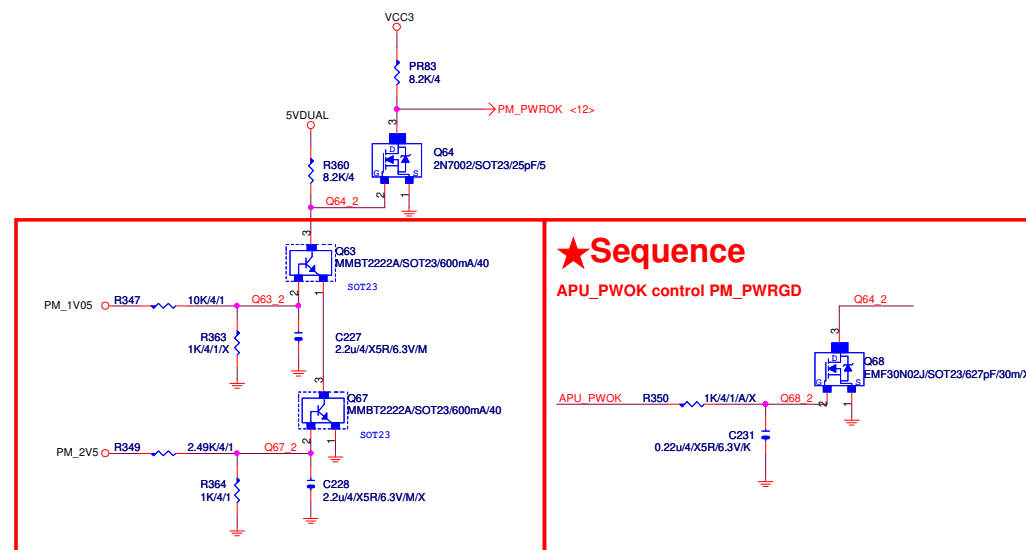
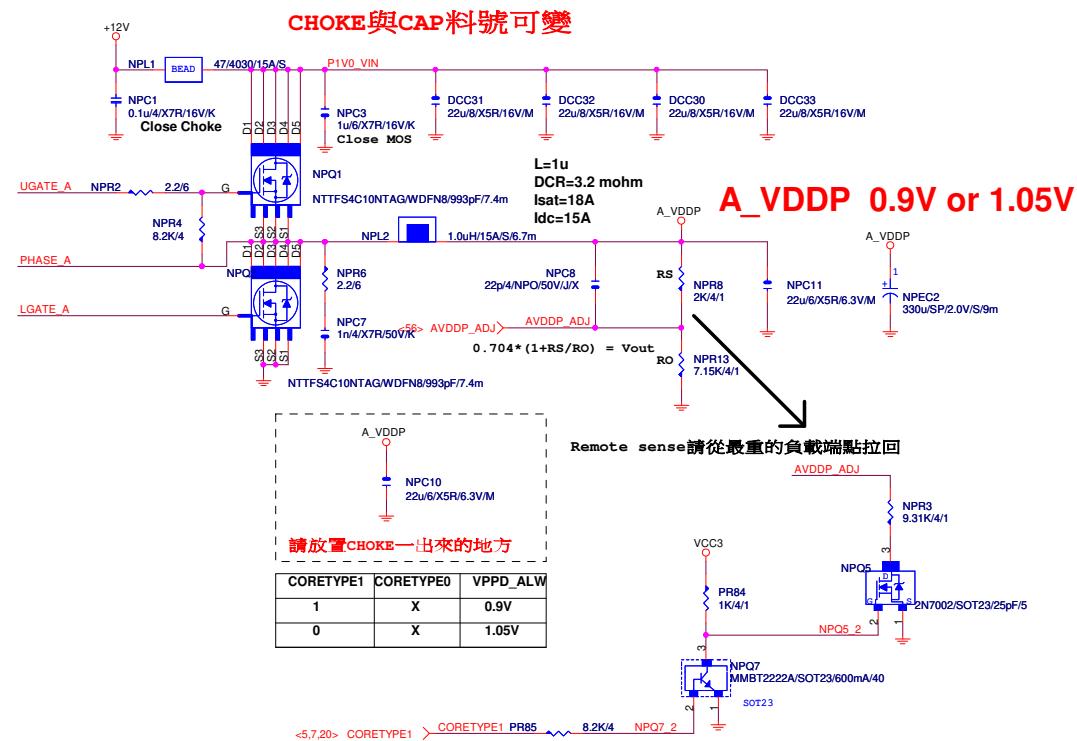
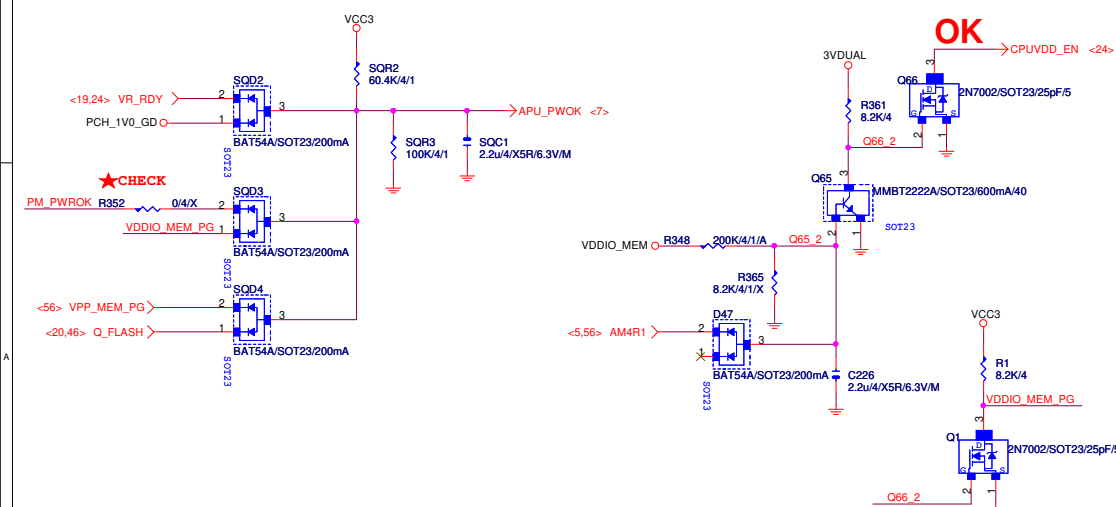
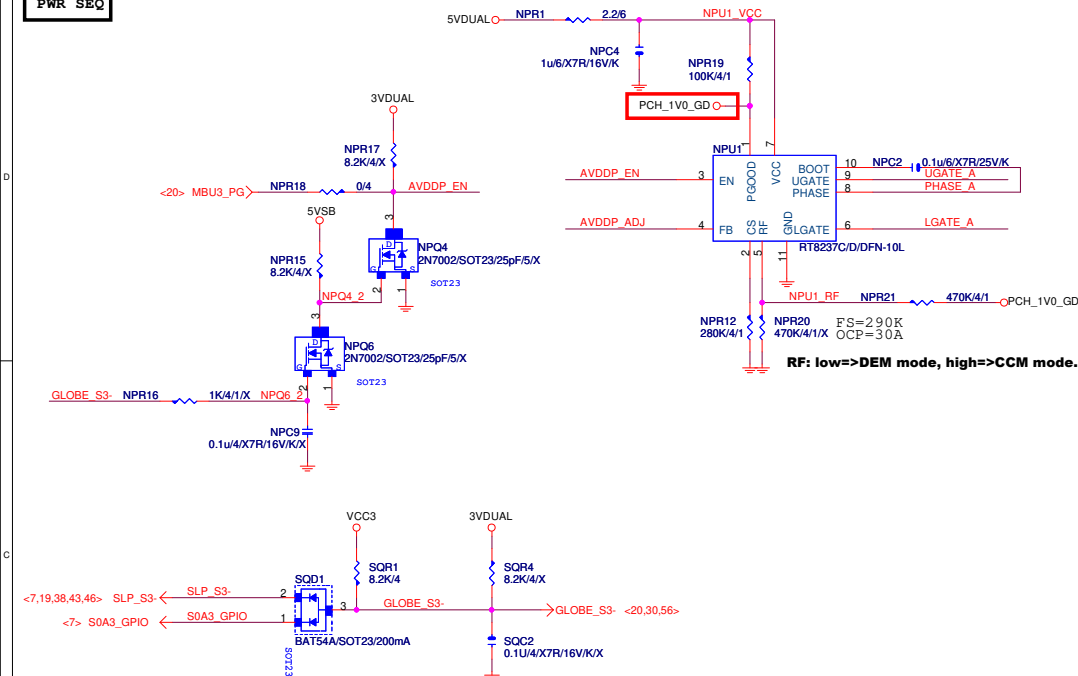


VCORE PHASE11_12



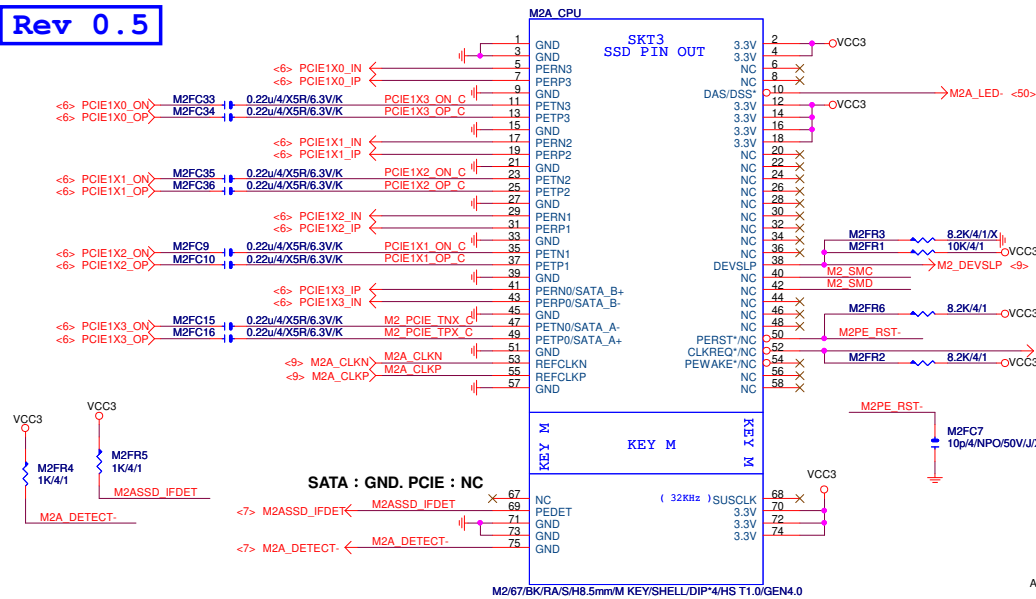
<24,25,26,28> TSEN1 << TSEN

[illegible]

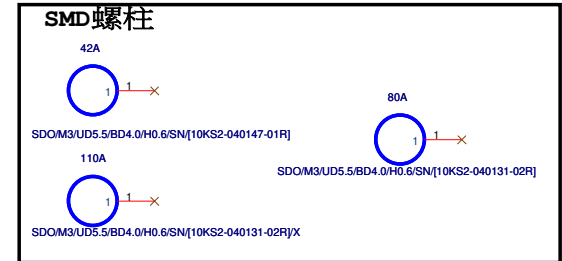
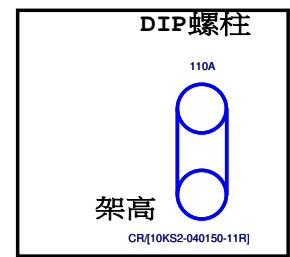
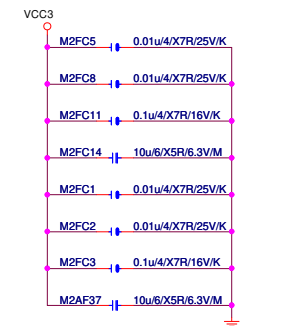




Rev 0.5

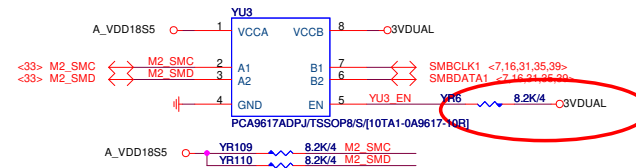
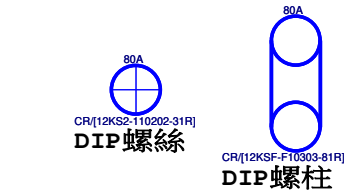


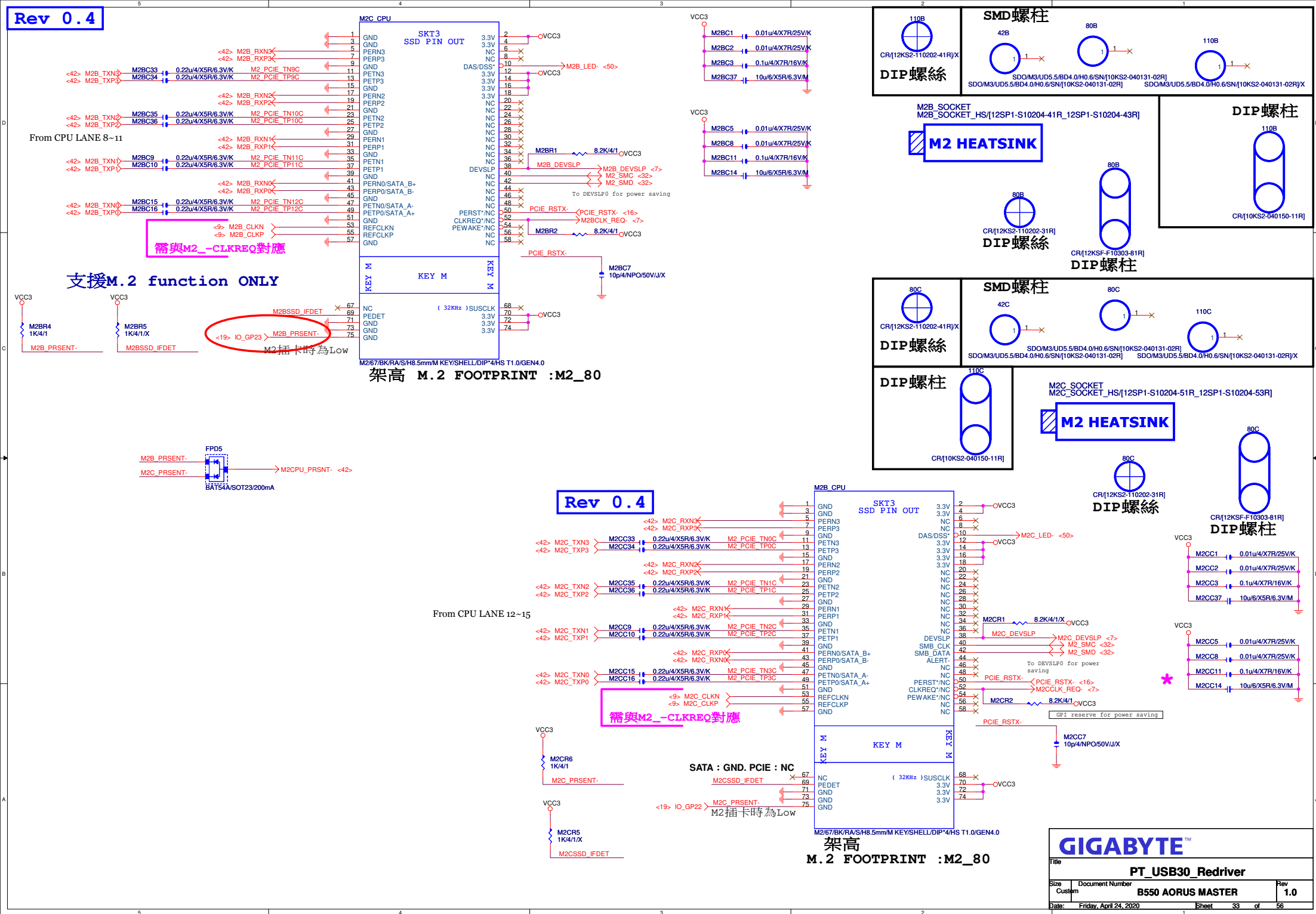
8.5H鐵殼
Footprint :M2_110(DIP)



M2A_SOCKET
M2A_SOCKET_HS [12SP1-S10204-31R_12SP1-S10204-33R]

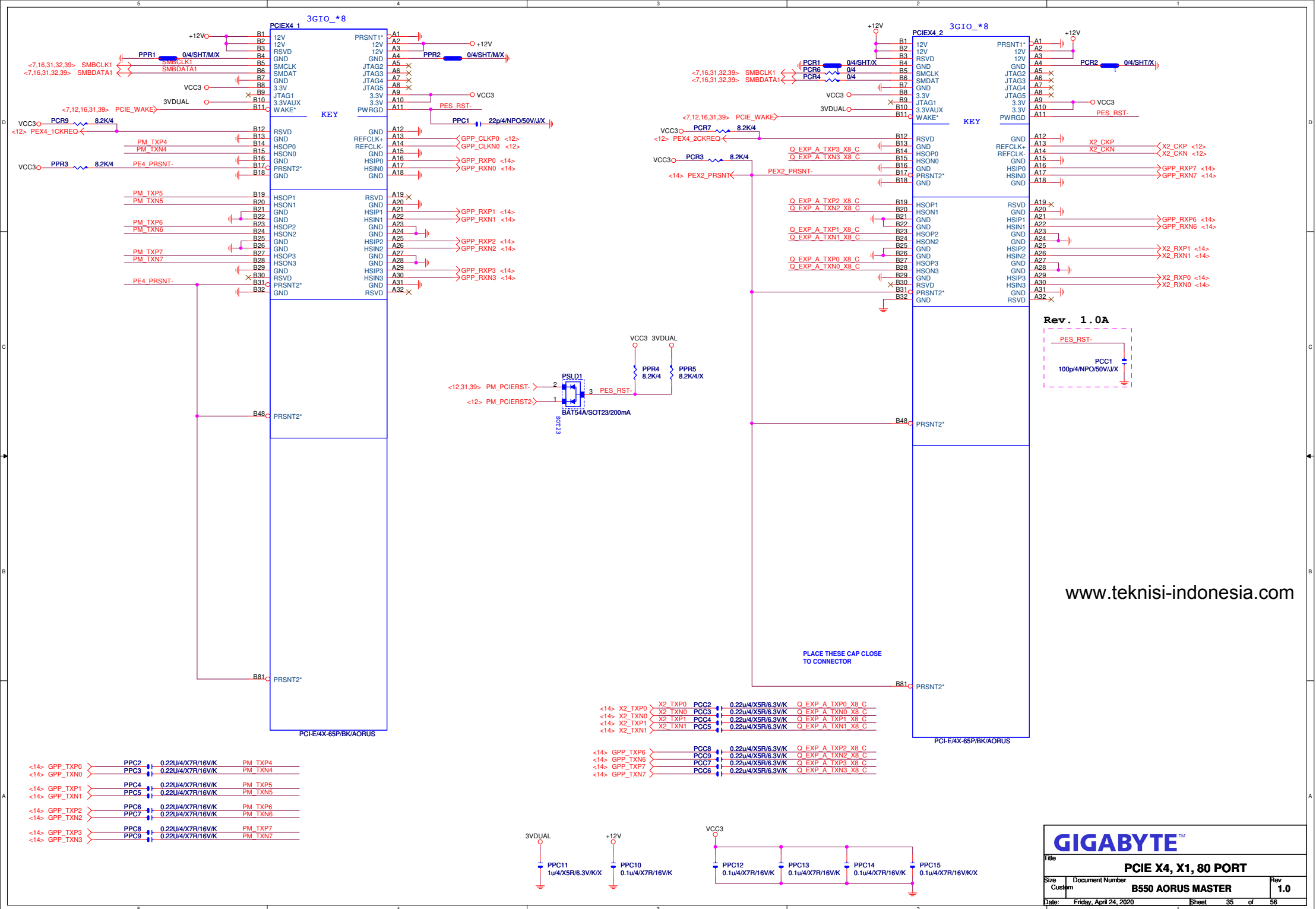
M2 HEATSINK



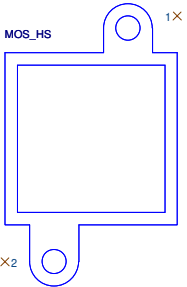
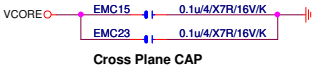
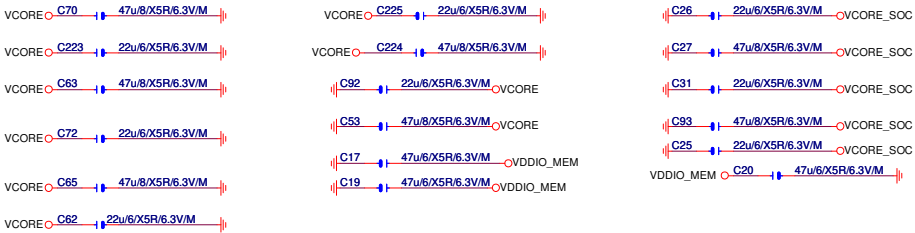


5	4	3	2	1
D				D
C				C
B				B
A				A

GIGABYTE™		
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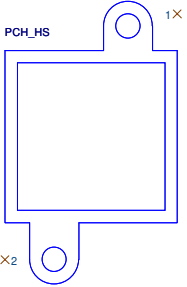


CPU TOP CAVITY



MOS_HS

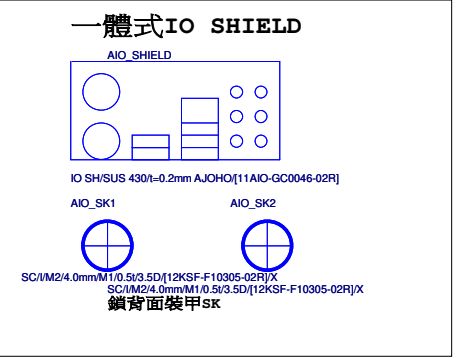
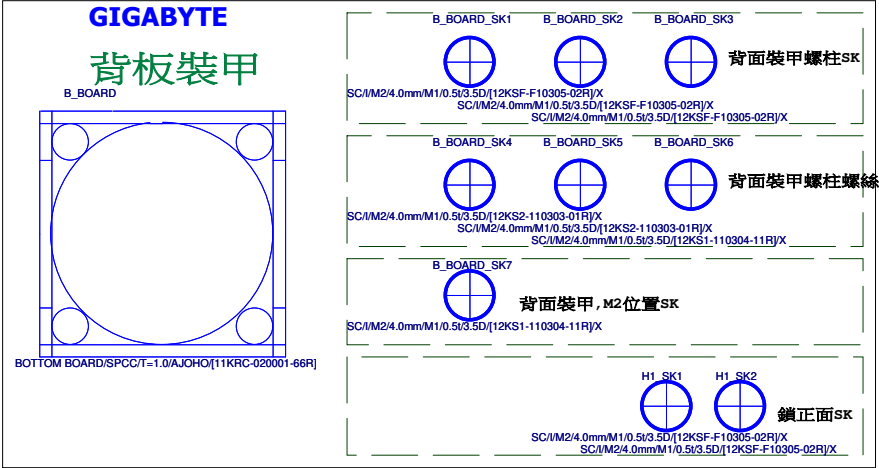
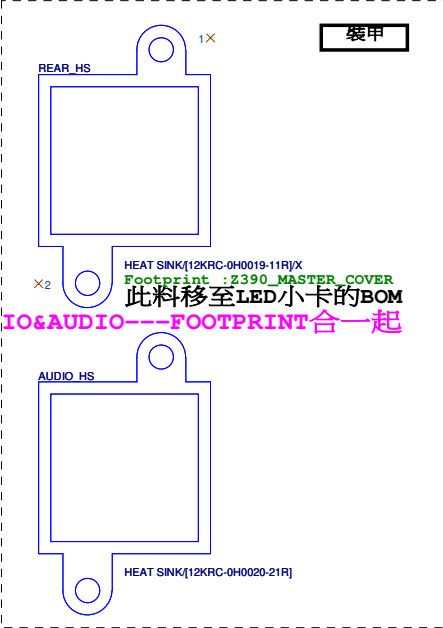
T+R
Footprint :
SINK_Z390_MASTER
HEAT SINK[12SP2-PAB55M-01R_12SP2-PAB55M-03R]



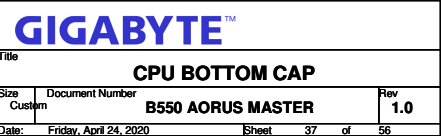
PCH_HS

Footprint :
SINK_Z390_MASTER_PCH
HEAT SINK[12SP2-S09013-01R_12SP2-S09013-03R]

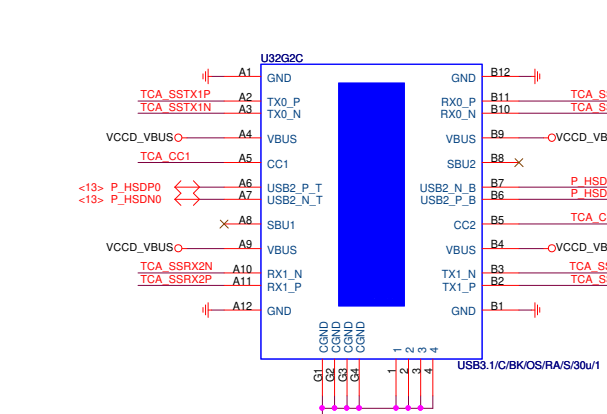
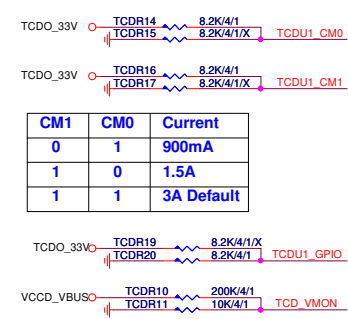
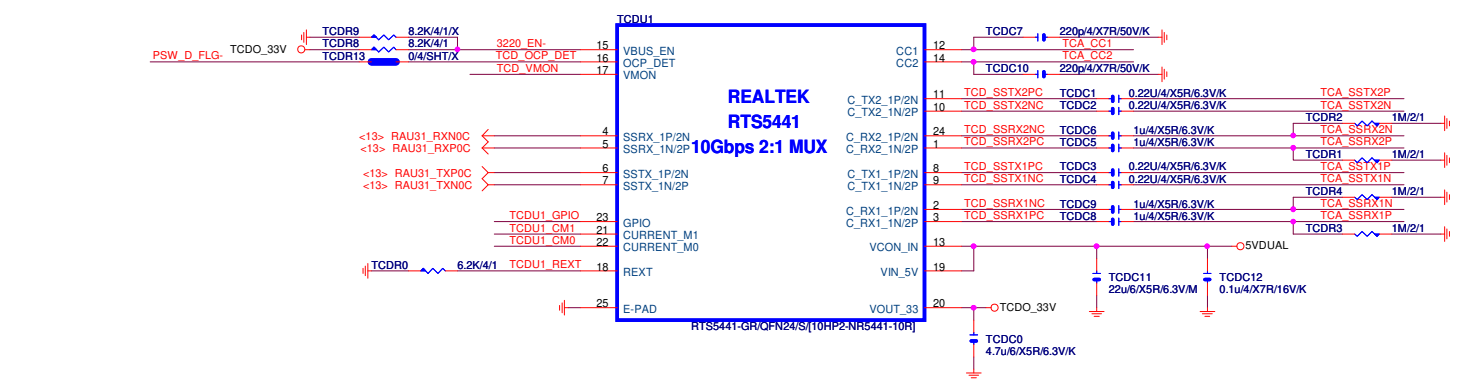
裝甲HEATSINK 分成四大部份



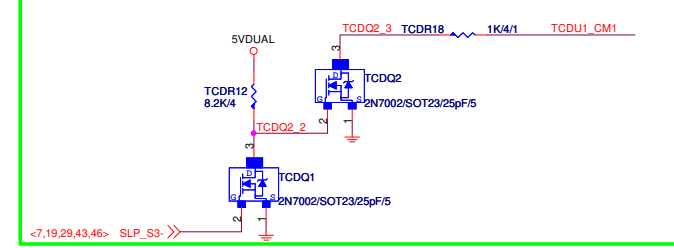
GIGABYTE™			
Title			
CPU TOP CAP			
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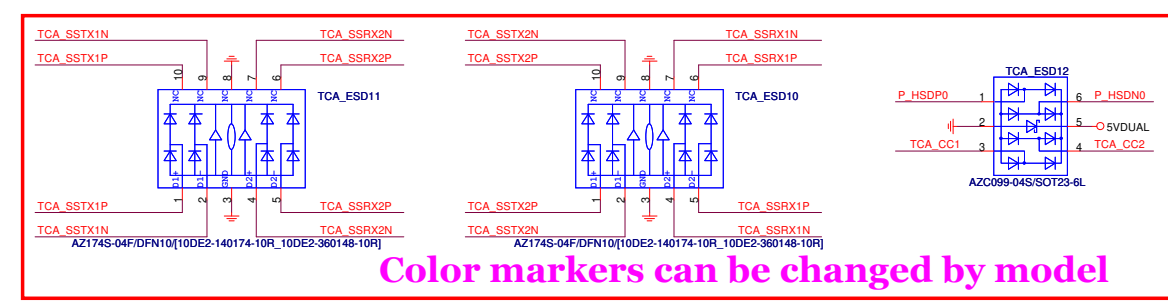
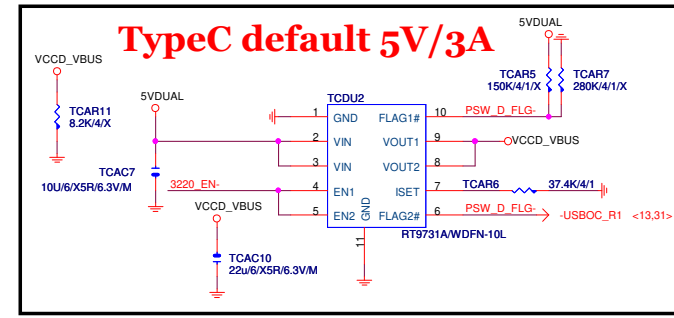
REALTEK CC LOGIC AND MUX RTS5441



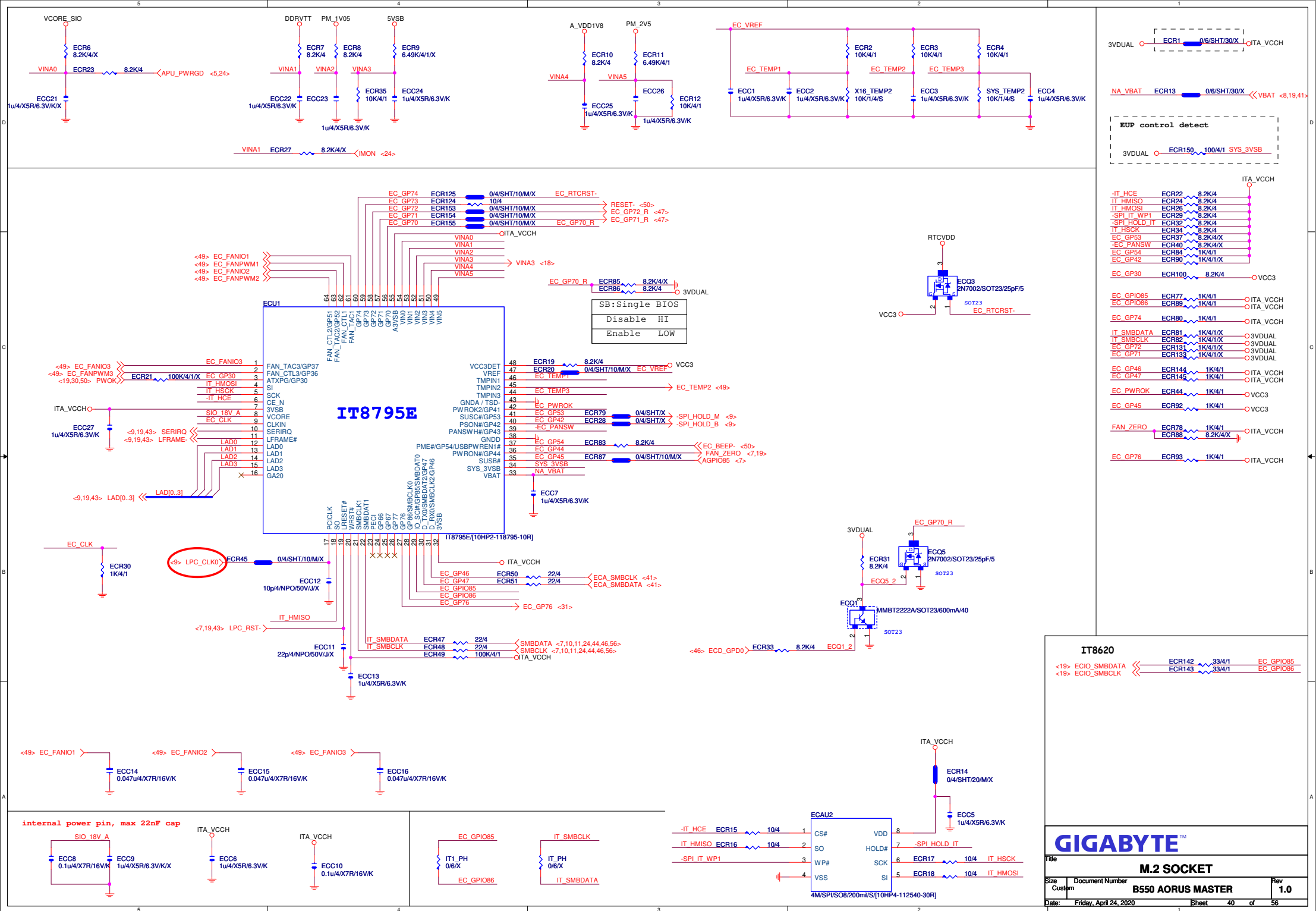
USB2.0 can be used the same source

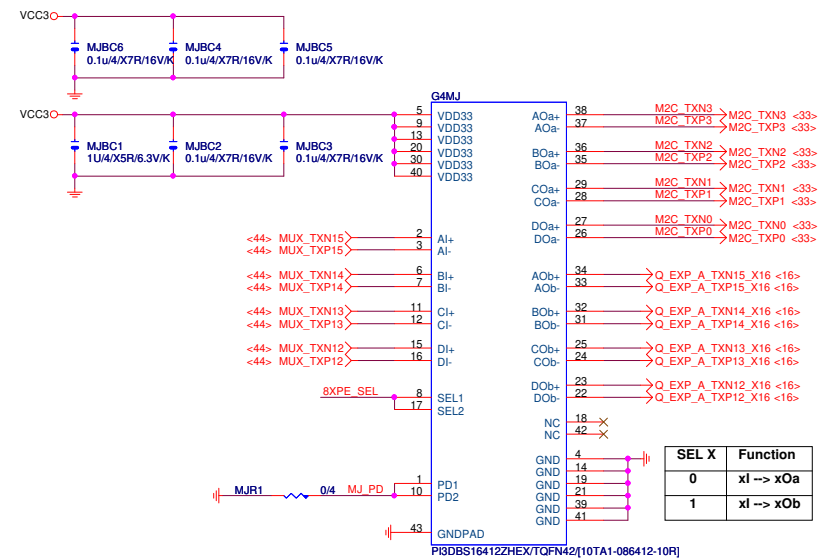
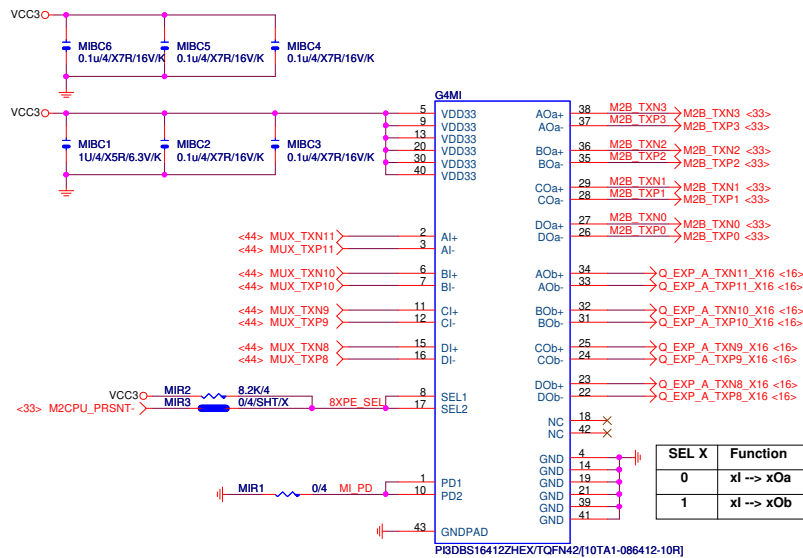


For VBUS current limit at 900mA on S3



Color markers can be changed by model



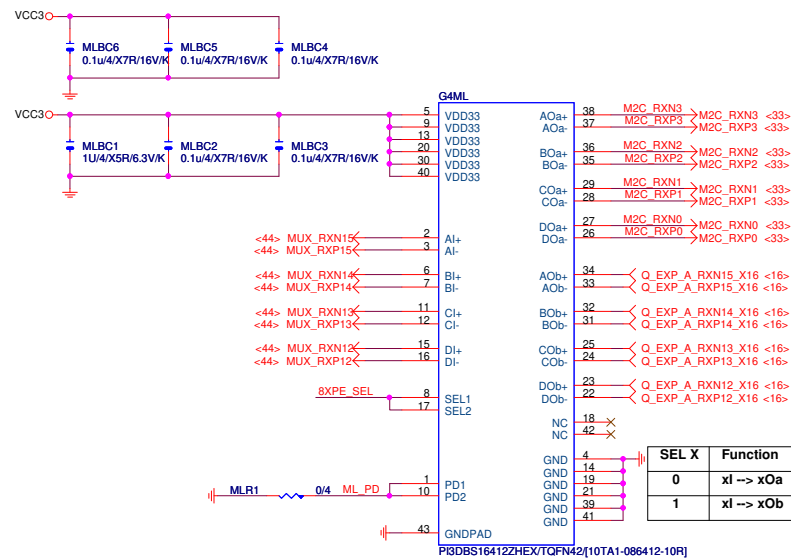
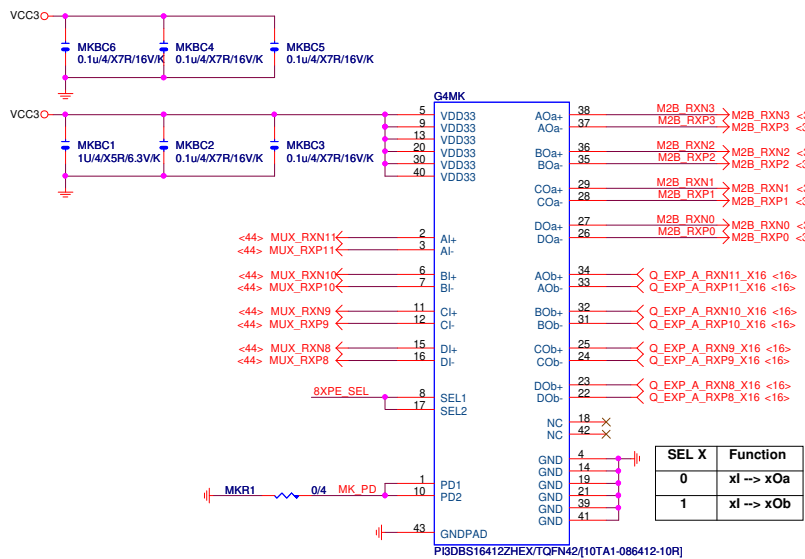


EXP_A_RXP[8..15] >>> EXP_A_RXP[8..15] <-6,44>

EXP_A_RXN[8..15] >>> EXP_A_RXN[8..15] <-6,44>

<-6,44> EXP_A_TXP[8..15] >>> EXP_A_TXP[8..15]

<-6,44> EXP_A_TXN[8..15] >>> EXP_A_TXN[8..15]

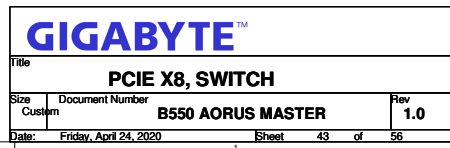
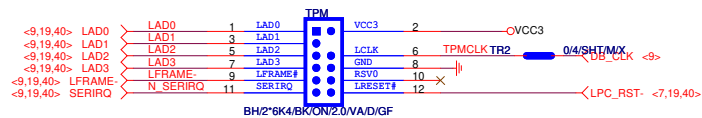
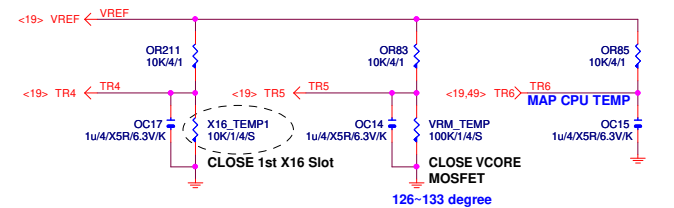


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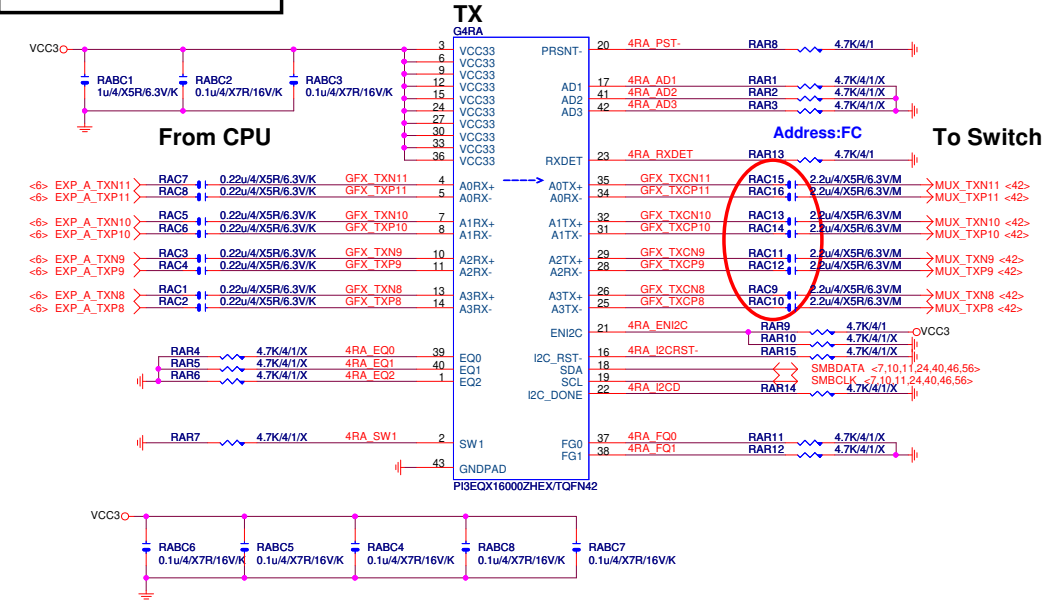
Title: **PCIE X8, SWITCH**

Size: Custom Document Number: **B550 AORUS MASTER** Rev: **1.0**

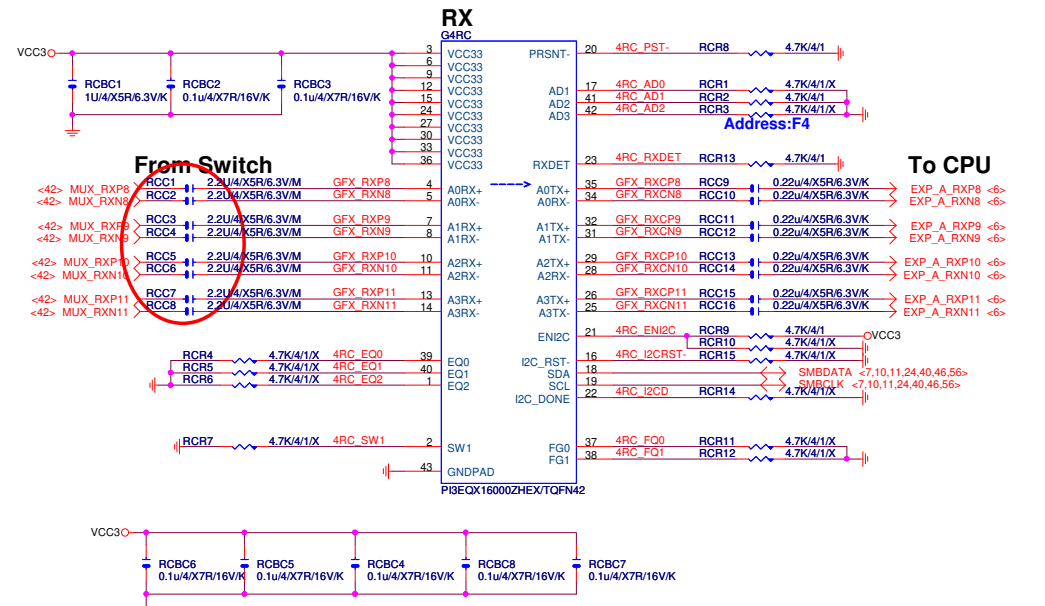
Date: Friday, April 24, 2020 Sheet: 42 of 56



PCIe GEN 4 REDRIVER



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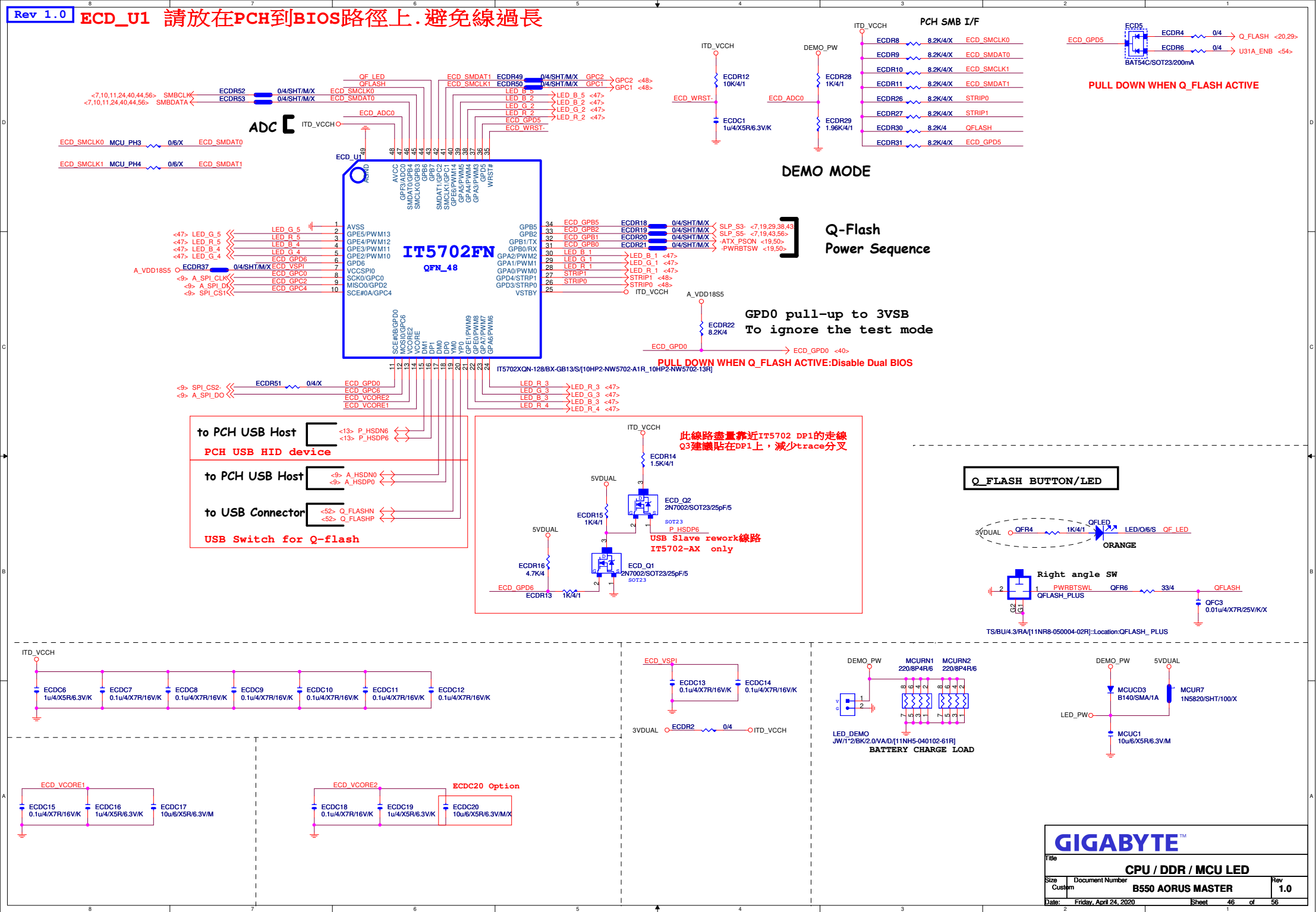
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Title			DIGITAL LED
Size	Document Number	Rev	
Custom	B550 AORUS MASTER	1.0	
Date:	Friday, April 24, 2020	Sheet	44 of 56

Rev: 0.1

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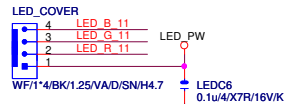
Title			ASM 2142 U31		
Size	Document Number				Rev
Custom	B550 AORUS MASTER				1.0
Date:	Friday, April 24, 2020			Sheet	45 of 56



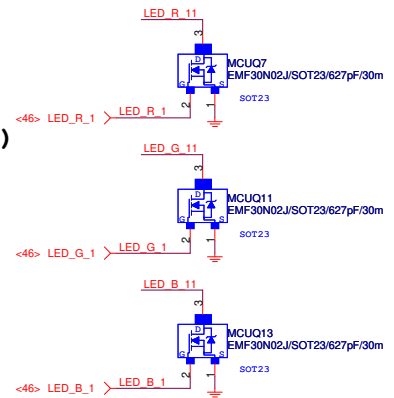
第一區 LED

第一區 LED CONTROL

FOR 後窗裝甲 led connect
(LED_COVER放在後窗裝甲內)



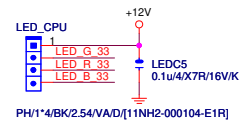
*Footprint : LED-1X4-1P25MM



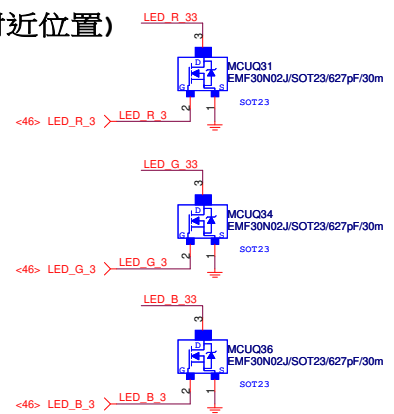
第三區 LED

第三區 LED CONTROL

燈條 LED (LED_CPU放在CPU附近位置)



Footprint "PH1X4-FAN-AMD-L"

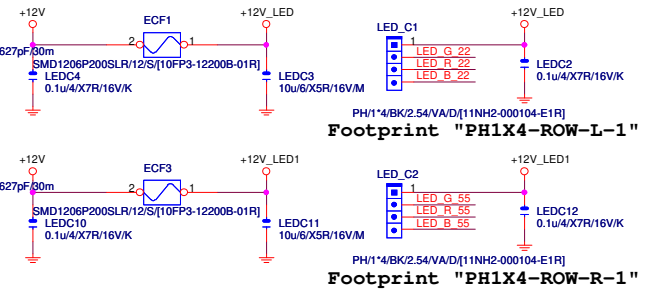
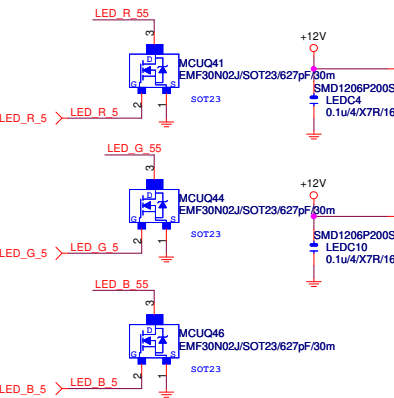
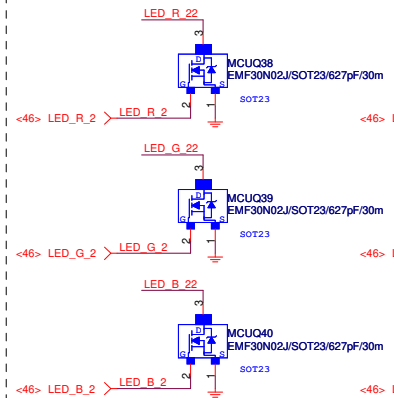


第五區 LED

第二區 LED CONTROL

第五區 LED CONTROL

燈條 LED (LED_C1放在PCB左邊板邊位置)
燈條 LED (LED_C2放在PCB右邊板邊位置)



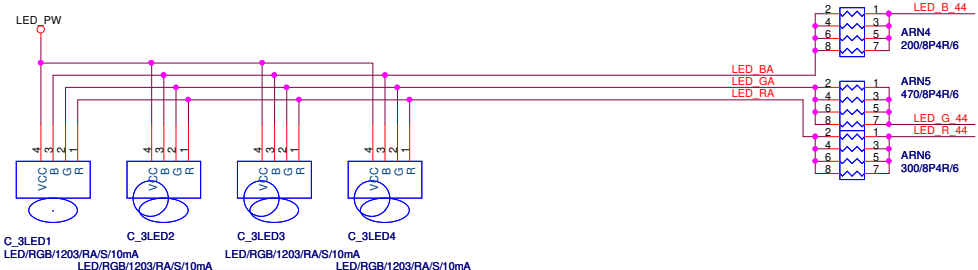
Footprint "PH1X4-ROW-L-1"

Footprint "PH1X4-ROW-R-1"

第四區 LED

第四區 LED CONTROL

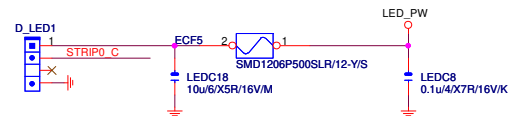
FOR AUDIO 正板測發光 LED*4 (位置在正板,依據AUDIO_HS設計擺放)



FOOTPRINT : LED-4P-RGB-SIDE-1

第六區 LED (靠近左上板邊位置)

Digital LED Strip1

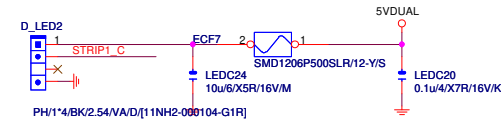


PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint PH1X4-CUT3-LED-L

第七區(靠近右下CPU板邊位置)

Digital LED Strip2

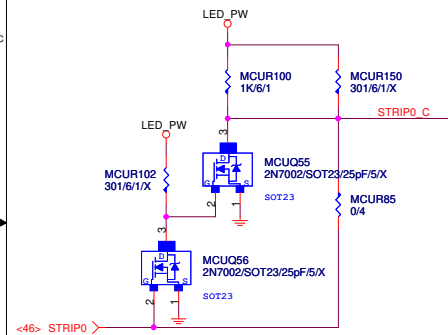


PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

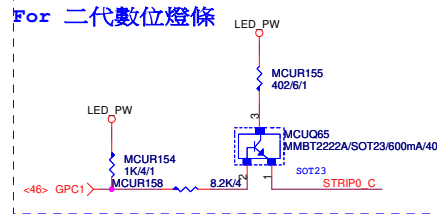
Footprint "PH1X4-CUT3-LED-R"

(for pin-name 與 model-name 同方向)

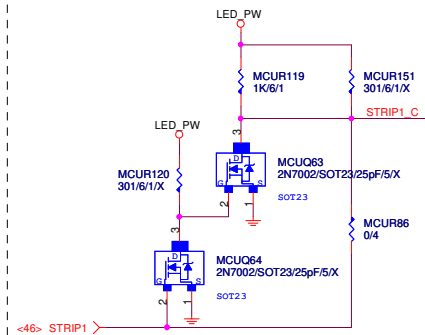
燈條 Level shift



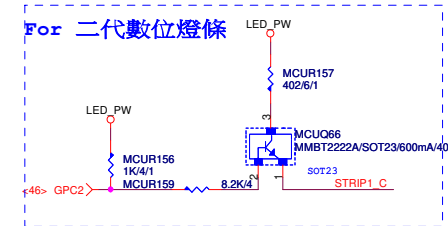
For 二代數位燈條



燈條 Level shift



For 二代數位燈條



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Title			
PCH / IO / HS / LED_C LED			
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Rev: 0.8 ★Update 2016.06.01

[illegible]

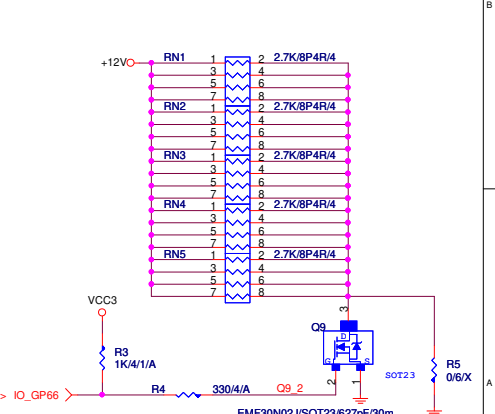
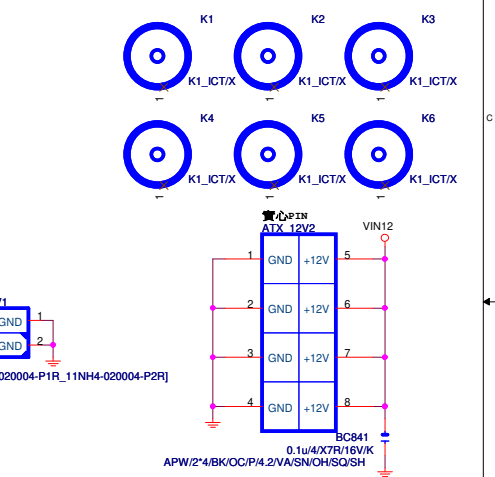
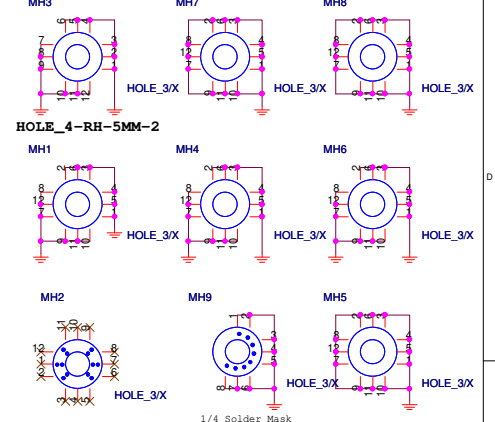
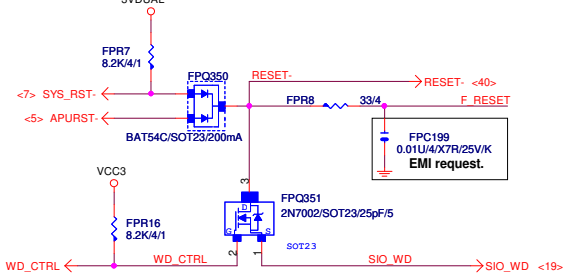
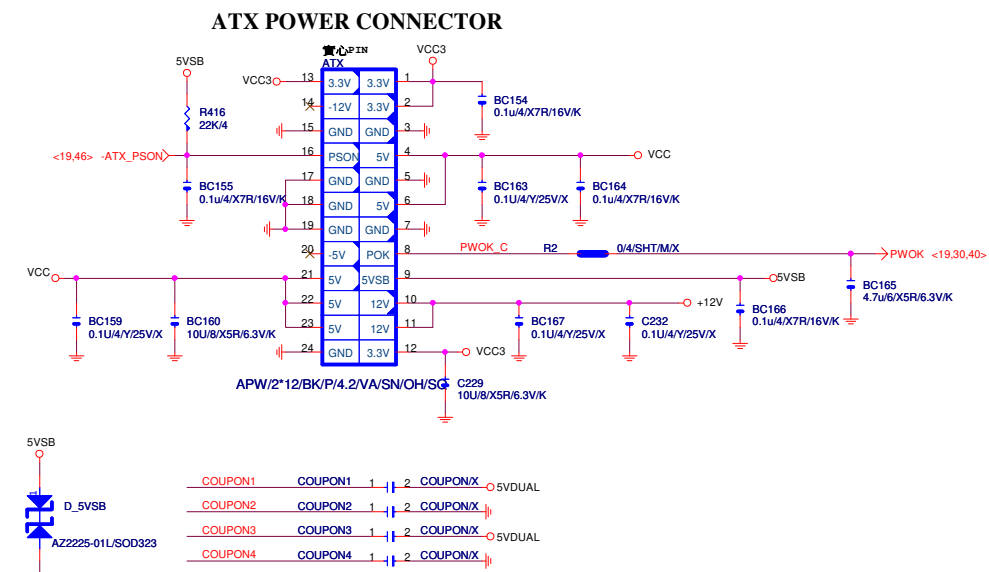
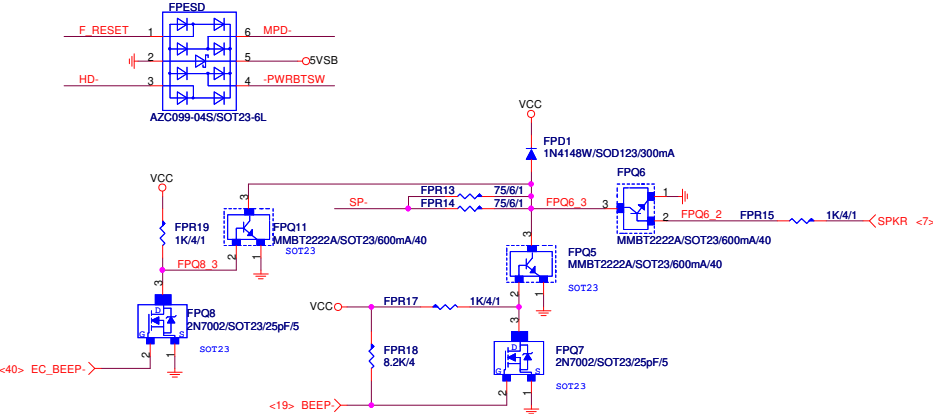
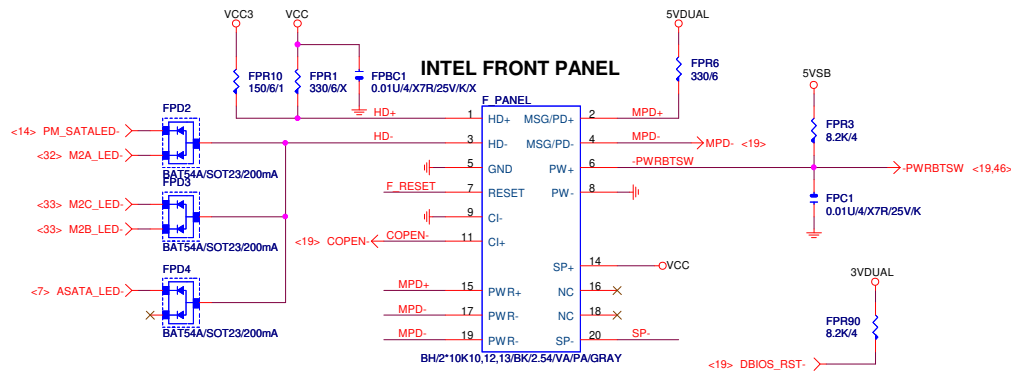
The schematic diagram illustrates the internal circuitry of the GIGABYTE PCIE X8, SWITCH module. The central component is the NCT3947S/ISOP8-EP controller, which is configured in MODE: Floating=> Auto mode, High=>PWM Mode, and Low=>Voltage Mode. The controller's pins are connected to various components:

- VIN** (Pin 2) is connected to **EC_FANPWM3** through a 1K4/1 resistor (FJR1).
- PWMOUT** (Pin 4) is connected to **FANJ_PWMOUT** through a 15K/4/1 resistor (FJR4).
- PWMIN** (Pin 3) is connected to **FANJ_PWMOUT** through a 15K/4/1 resistor (FJR4).
- DCIN** (Pin 8) is connected to **FANJDCIN** through a 100K/4/1 resistor (FJR2).
- MODE** (Pin 6) is connected to **FANJ_MODE** through a 0.1u4/4/1 capacitor (FJC1).
- NC** (Pin 7) is connected to **FANJ_VOUT** through a 15K/4/1 resistor (FJR4).
- PGND** (Pin 9) is connected to **FANJ_VOUT** through a 15K/4/1 resistor (FJR4).
- FANJ_VOUT** (Pin 1) is connected to **FANJ_VOUT** through a 15K/4/1 resistor (FJR4).
- FANJ_VOUT** (Pin 1) is connected to **FANJ_VOUT** through a 15K/4/1 resistor (FJR4).
- FANJ_VOUT** (Pin 1) is connected to **FANJ_VOUT** through a 15K/4/1 resistor (FJR4).

The diagram also shows the connection to the **EC_FANPWM3** signal and the **FANJ_VOUT** signal. The module is labeled **GIGABYTE** and **PCIE X8, SWITCH**.

Title			
PCIE X8, SWITCH			
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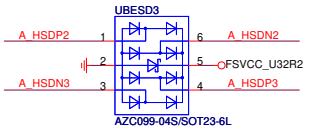
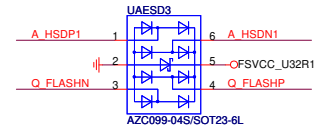
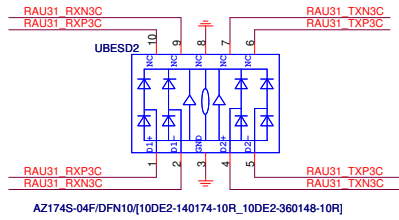
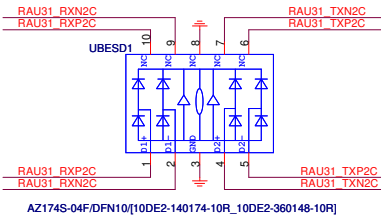
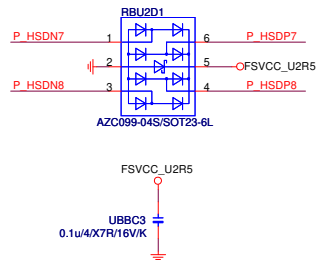
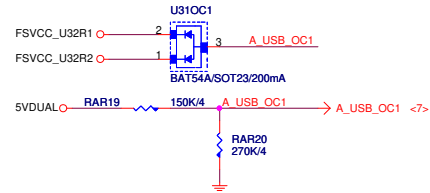
KBL FAN LOCATION MAP REFER TO PAGE.27



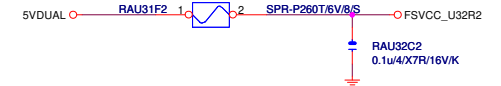
GIGABYTE		
Title: ATX, FRONT PANEL		
Size: Custom	Document Number: B550 AORUS MASTER	Rev: 1.0
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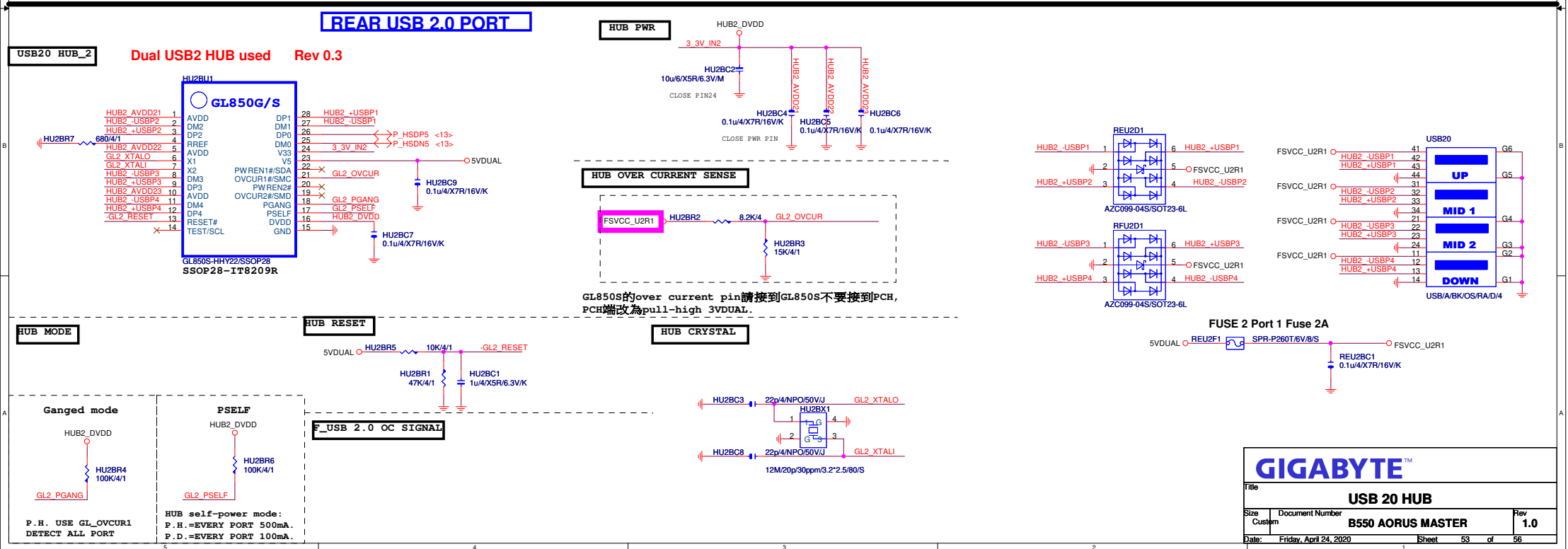
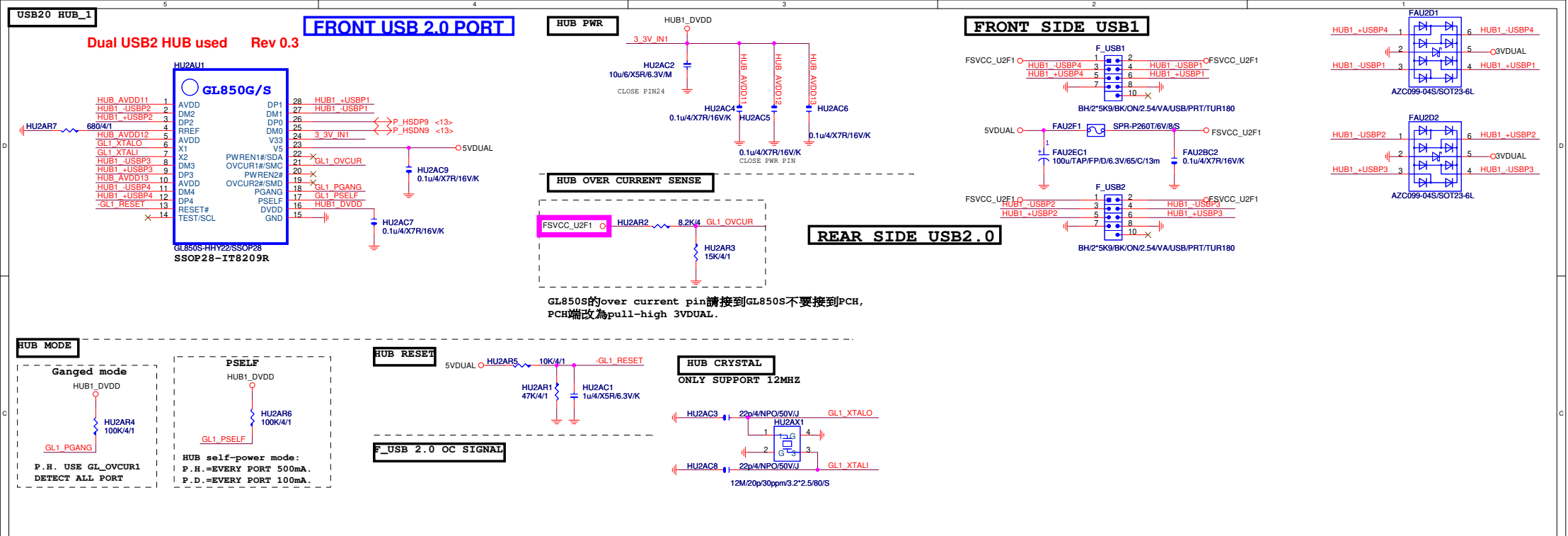
5	4	3	2	1
D				D
C				C
B				B
A				A

GIGABYTE™		
Title Realtek RTL8125		
Size Custom	Document Number B550 AORUS MASTER	Rev 1.0
Date: Friday, April 24, 2020	Sheet 1	51 of 56

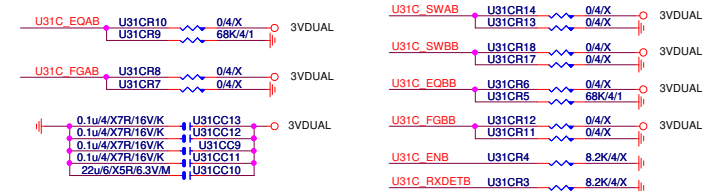


CONNECTOR料號要改



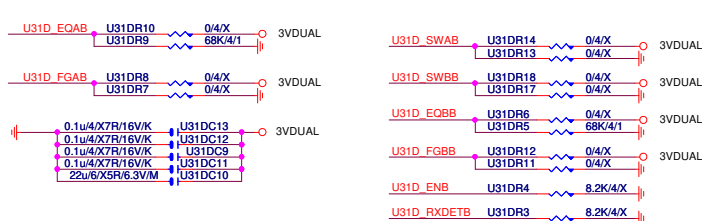


CPU

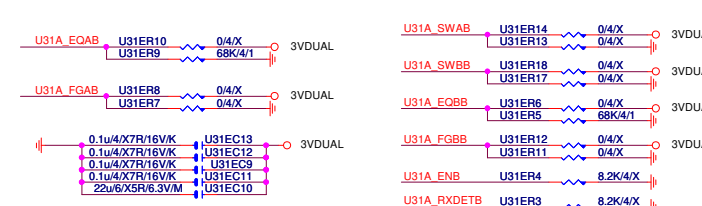


1. Differential Pair can't be swaped
2. Redriver to Connector Length min. 500mil

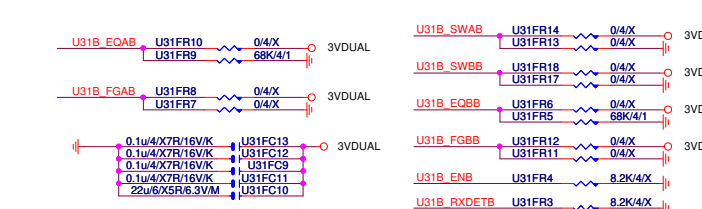
CPU



CPU



CPU

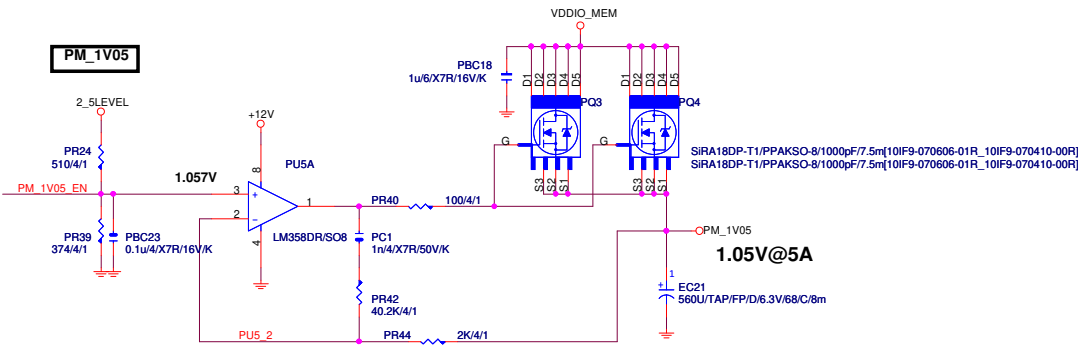


Title			
PI3EQX1002B Redriver/DC			
Size	Document Number	Rev	
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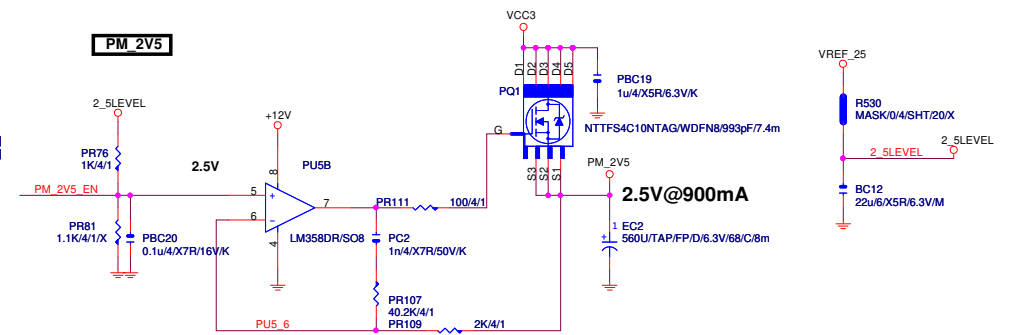


GIGABYTE™			
Title X570 POWER			
Size Custom	Document Number B550 AORUS MASTER		Rev 1.0
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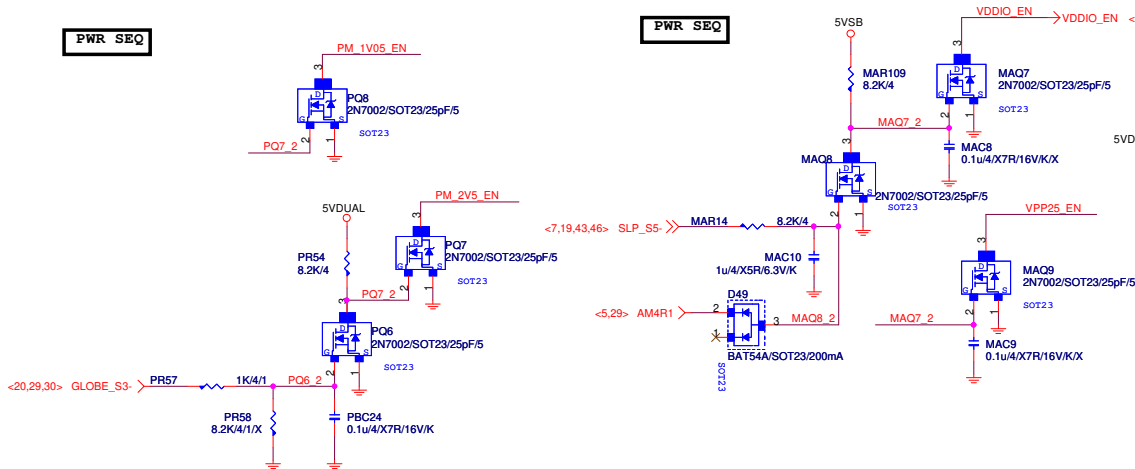
PM_1V05



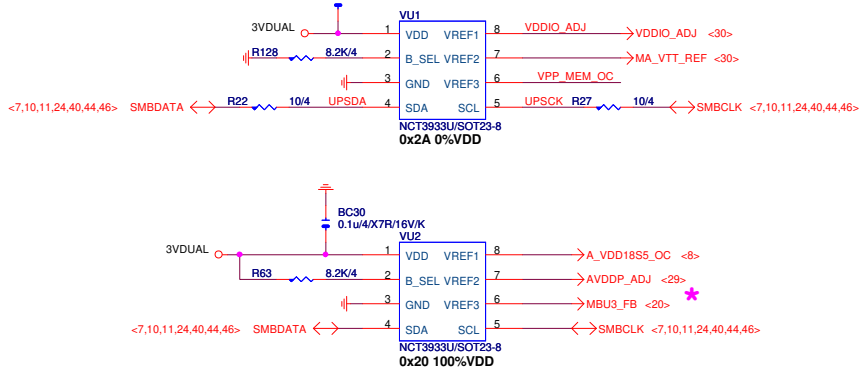
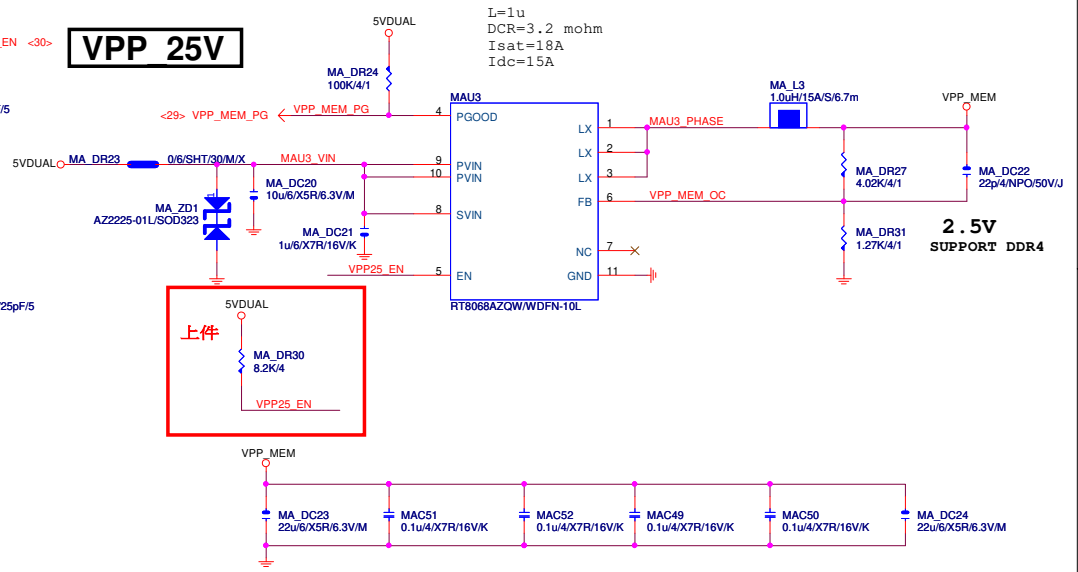
PM_2V5



PWR_SEQ



VPP 25V



Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting

GIGABYTE

Title				PM POWER	
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